CORONA
REV 1.01
FAB E
XDK 4L

H103358
REV A

RULES: (APPLIED WHEN POSSIBLE)
1.) MSB TO LSB IS TOP TO BOTTOM
2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7.) SUFFIX V_ IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12.) SUFFIX _P FOR P JUNCTION
13.) SUFFIX _EN FOR ENABLE
14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15.) PWRGD FOR POWER GOOD
16.) REV AND FAB ARE SET USING CUSTOM VARIABLES. TOOLS>OPTIONS>VARIABLES

[PAGE_TITLE=COVER PAGE]

DRAWING
Thu Feb 17 21:37:16 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	1/87	E	1.01

GCPU SETUP

25 IN CPU_RST_N
FT3T10 FTP 1
R4P5 2 1 1.27 KOHM 1% 402 CH
CPU_RST_V1P1_N OUT 63
1 C5R11 360 PF 5% 50 V 2 EMPTY 603
1 R4P4 2 KOHM 1% 2 CH 402

FT3T11 FTP 1
25 IN CPU_PWRGD
1 R3E10 10 KOHM 5% 2 CH 402
1 C5R66 360 PF 5% 50 V 2 EMPTY 603

U5E1 14 OF 17 IC
GCPU VERSION 1
D5 HARD_RESET_B
CHECKSTOP_B E5 → CPU_CHECKSTOP_N OUT 63
T5 POWER_GOOD

22 IN CPU_CLK_DP
R4D1 2 1 0 OHM 5% 402 CH
IN CPU_CLK_DP_R2 → P2 CPU_CLK_DP

22 IN CPU_CLK_DN
R4D2 2 1 0 OHM 5% 402 CH
IN CPU_CLK_DN_R2 → P1 CPU_CLK_DN

V_CPUCORE
I112
1 R4R22 100 OHM 5% 2 EMPTY 402
1 R4R23 100 OHM 5% 2 EMPTY 402
I113 1 DB4R3
I114 1 DB4R2

CPU_DBG_RST_EN	INTERNAL PULLDN
GPU_DBG_RST_EN	INTERNAL PULLDN

CPU_DBG_RST_EN → P5 CPU_DBG_RST_EN<DN>
GPU_DBG_RST_EN → R5 GPU_DBG_RST_EN<DN>

OUT EDRAM_PSRO_DOUT → N6 PSRO_DOUT
OUT CPU_PSRO0_OUT → G7 PSRO0_OUT

VID6 C24 → CPU_VREG_APS6 OUT 43
VID5 B24 → CPU_VREG_APS5 OUT 43
VID4 A24 → CPU_VREG_APS4 OUT 43
VID3 C23 → CPU_VREG_APS3 OUT 43
VID2 B23 → CPU_VREG_APS2 OUT 43
VID1 A23 → CPU_VREG_APS1 OUT 43
1 FTP FT7P8
1 FTP FT7P7
1 FTP FT7P6
1 FTP FT7P5
1 FTP FT7P4
1 FTP FT7P3

V_CPUPLL
WHEN V_CPUPLL=1.83V
SET VGATE=1.20V
ACTUAL=1.202V
N: IF V_CPUPLL CHANGES
VGATE RESISTORS SHOULD BE ADJUSTED
1 R5T8 562 OHM 1% 2 CH 402
CPU_VGATE → V6 V_GATE

1 R5T9 1.07 KOHM 1% 2 CH 402

<DN>PULSE_LIMIT_BYPASS J6 → CPU_LIMIT_BYPASS OUT
<DN>PLL_BYPASS F8 → CPU_PLL_BYPASS OUT

OUT RESISTOR0_DP → L7 RESISTOR0_DP
OUT RESISTOR0_DN → M7 RESISTOR0_DN
SRVID A3 → CPU_SRVID OUT 51
EFU_POWERON C1 → VREG_EFUSE_EN OUT 52

OUT CPU_EXT_CLK_EN → F7 EXT_CLK_EN<DN>

CPU_TINIT → J7 TI_39_TINIT
CPU_TE → E7 TE
CORE_HF_BGR_PLL M6 → CORE_HF_BGR_PLL OUT

1 R4R21 200 OHM 5% 2 CH 402
1 R4R20 200 OHM 5% 2 CH 402

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6 LAYER ONLY SIGNALS

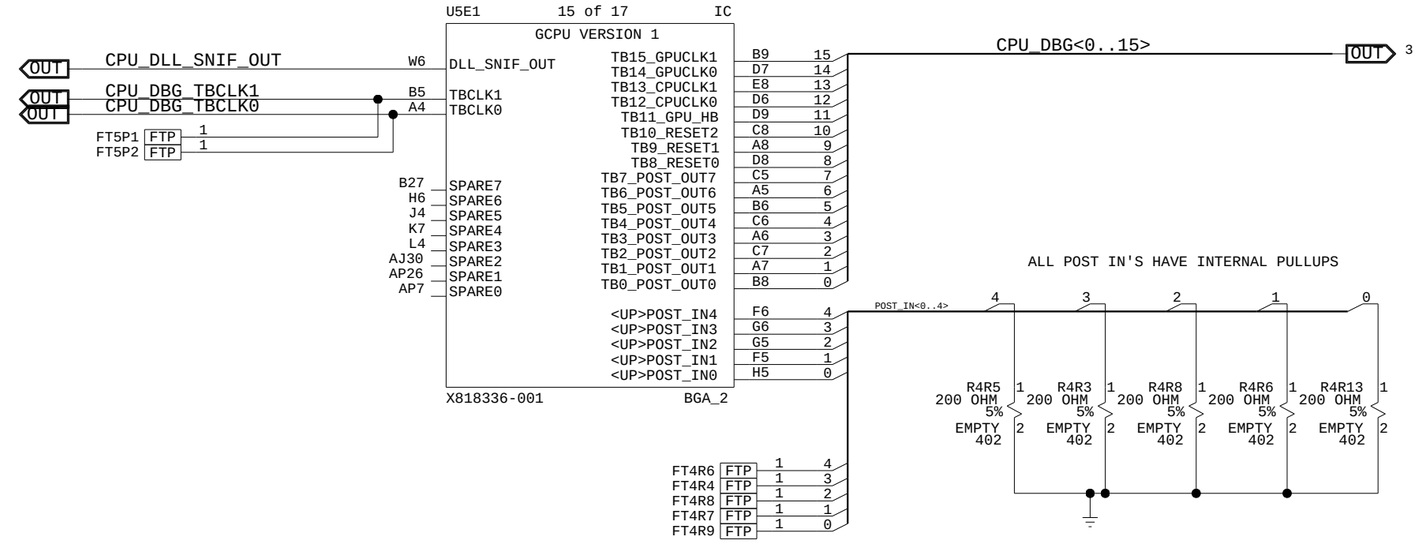
CORE_HF_BGR_PLL	6 LAYER ONLY; TP ONLY
CPU_LIMIT_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_PLL_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_CORE_HF_CLKOUT_DN	6 LAYER ONLY; TP ONLY
CPU_CORE_HF_CLKOUT_DP	6 LAYER ONLY; TP ONLY
CPU_EXT_CLK_EN	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_DLL_SNIF_OUT	6 LAYER ONLY; TP ONLY
CPU_VDDS0_DP	6 LAYER ONLY
CPU_VDDS0_DN	6 LAYER ONLY
CPU_VDDS1_DP	6 LAYER ONLY
CPU_VDDS1_DN	6 LAYER ONLY
RESISTOR0_DP	6 LAYER ONLY
RESISTOR0_DN	6 LAYER ONLY
EDRAM_PSRO_DOUT	6 LAYER ONLY

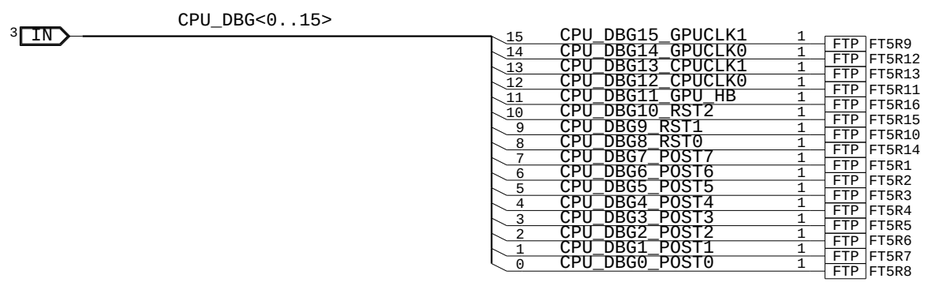
[PAGE_TITLE=GCPU SETUP]

DRAWING
Thu Feb 17 10:12:25 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	2/87	E	1.01

GCPU, DEBUG BUS



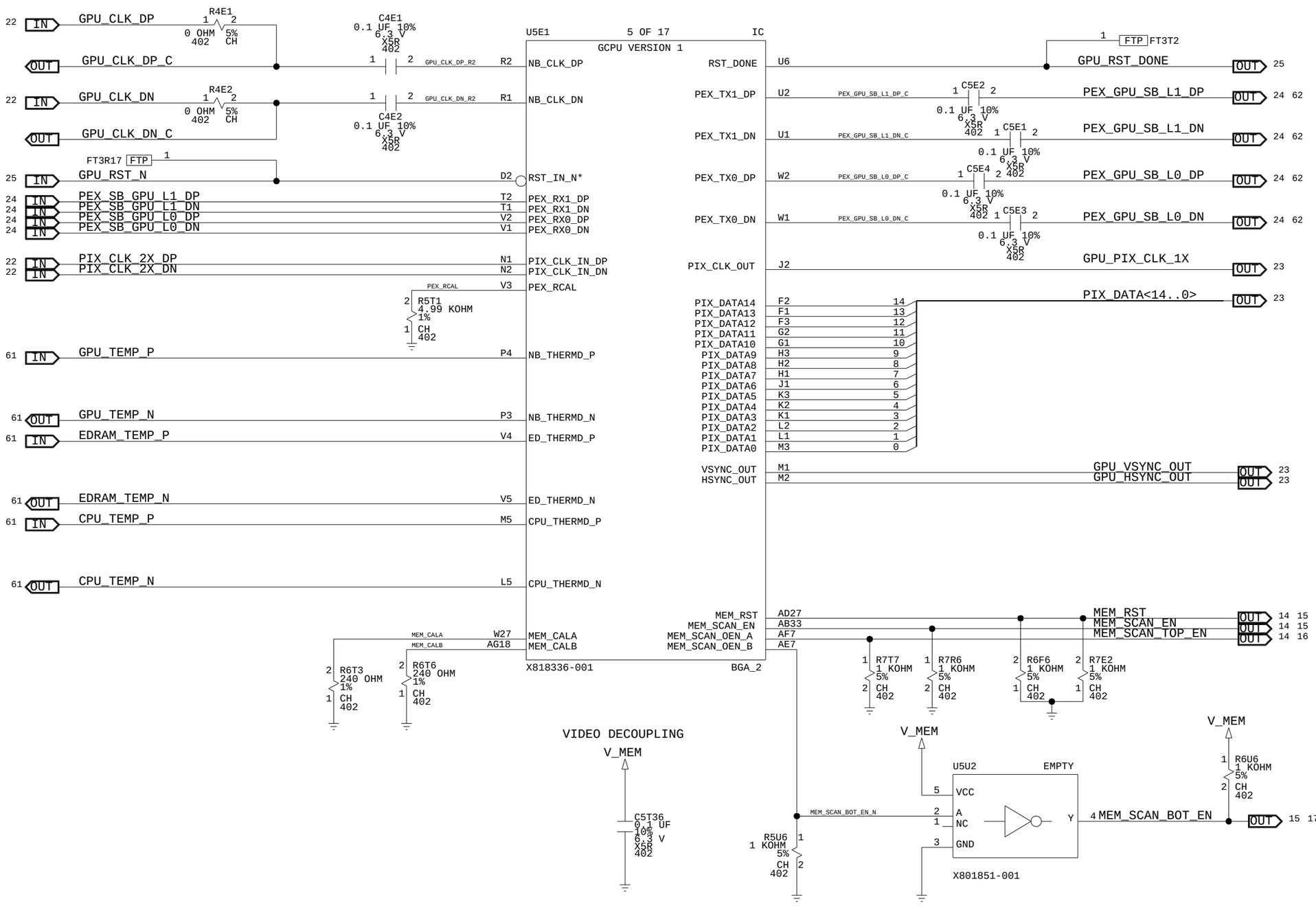


[PAGE_TITLE=GCPU, DEBUG BUS]

DRAWING
Thu Feb 17 10:12:25 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	3/87	E	1.01

GCPU, VIDEO + PCIEX

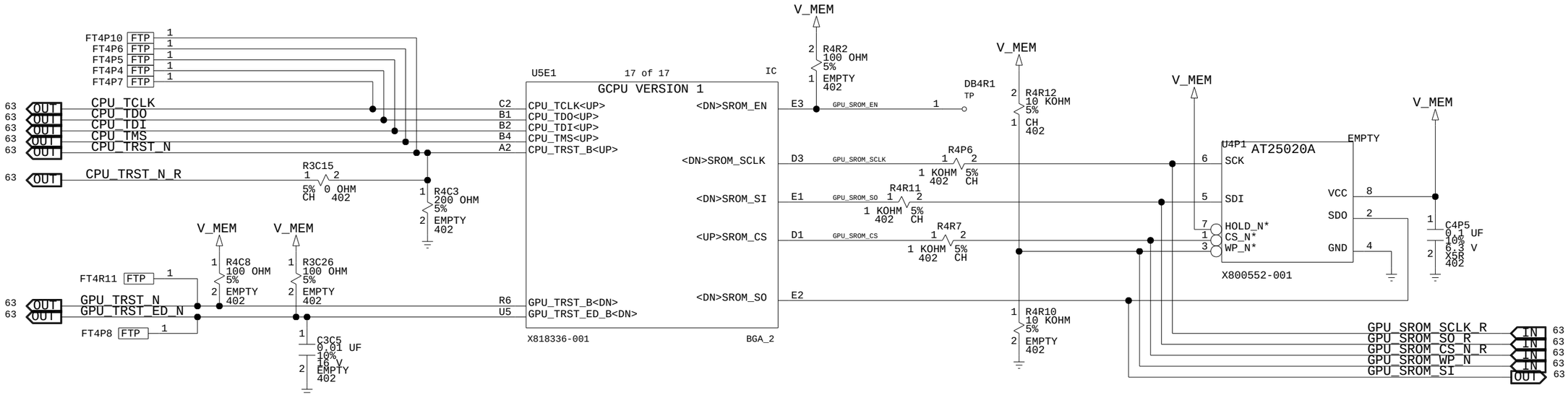


[PAGE_TITLE=GCPU, VIDEO + PCIEX]

DRAWING
Thu Feb 17 10:12:25 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	4/87	E	1.01

GCPU, EEPROM + JTAG



[PAGE_TITLE=GCPU, EEPROM + JTAG]

DRAWING
Thu Feb 17 10:12:26 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	5/87	E	1.01

GCPU, PLL POWER + FSB POWER

V_GPUPCIE V_CPUEDRAM V_CPUPLL V_EFUSE

U5E1 16 of 17 IC

GCPU VERSION 1

CPU_VDDS1_DP (OUT) CPU_VDDS1_DP (OUT) → H25 VDDS1_DP, J26 VDDS1_DN

CPU_VDDS0_DP (OUT) CPU_VDDS0_DN (OUT) → P7 VDDS0_DP, N7 VDDS0_DN

E4 VDDE

CORE_HF_CLKOUT_DP L6 → CPU_CORE_HF_CLKOUT_DP (OUT)

CORE_HF_CLKOUT_DN K6 → CPU_CORE_HF_CLKOUT_DN (OUT)

FB5R1	V_CPU_PVDDA_MEM	D4	PVDDA_MEM
ST5R1	V_CPU_PVSSA_MEM	C4	PVSSA_MEM
FB5T2	V_CPU_PVDDA_PEX	U3	PVDDA_PEX
ST5T1	V_CPU_PVSSA_PEX	U4	PVSSA_PEX
FB5R2	V_CPU_PVDDA_HS	C3	PVDDA_HS
ST5R2	V_CPU_PVSSA_HS	B3	PVSSA_HS
FB5T3	V_CPU_PVDDA_ED	W5	PVDDA_ED
ST5T2	V_CPU_PVSSA_ED	W4	PVSSA_ED
FB5R5	V_CPU_VDDA_RNG	N4	VDDA_RNG
ST5R5	V_CPU_GNDA_RNG	N3	GNDA_RNG
FB5R4	V_CPU_CORE_HF_VDDA_PLL	J5	CORE_HF_VDDA_PLL
ST5R4	V_CPU_CORE_HF_GNDA_PLL	K5	CORE_HF_GNDA_PLL
FB5R3	V_GPU_VDDA_PLL	G4	GPU_VDDA_PLL
ST5R3	V_GPU_GNDA_PLL	H4	GPU_GNDA_PLL
		R3	VDD_VTT
FB5T1	V_CPU_VDD_VTTA	R4	VDD_VTTA

FB 603 0.2A 0.5 DCR

C5R14 C5T9 C5R17 C5R54 C5R42 C5R31 10 UF 20% 6.3 V X5R 805

C5T13 4.7 UF 10% 6.3 V X5R 603

C5I4 4.7 UF 10% 6.3 V X5R 603

C5I6 0.1 UF 10% 6.3 V X5R 402

SHORT

DB5R5

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DRAWING

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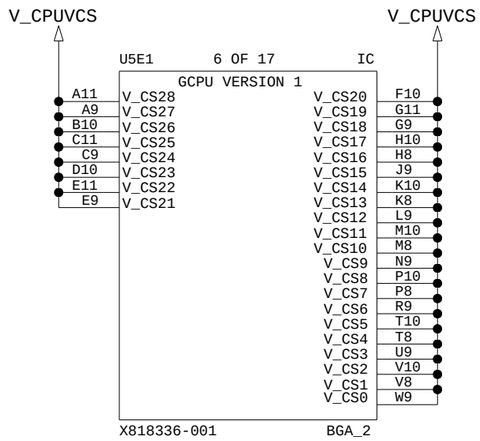
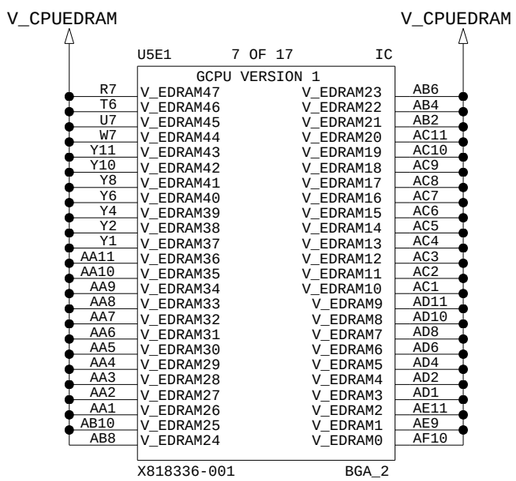
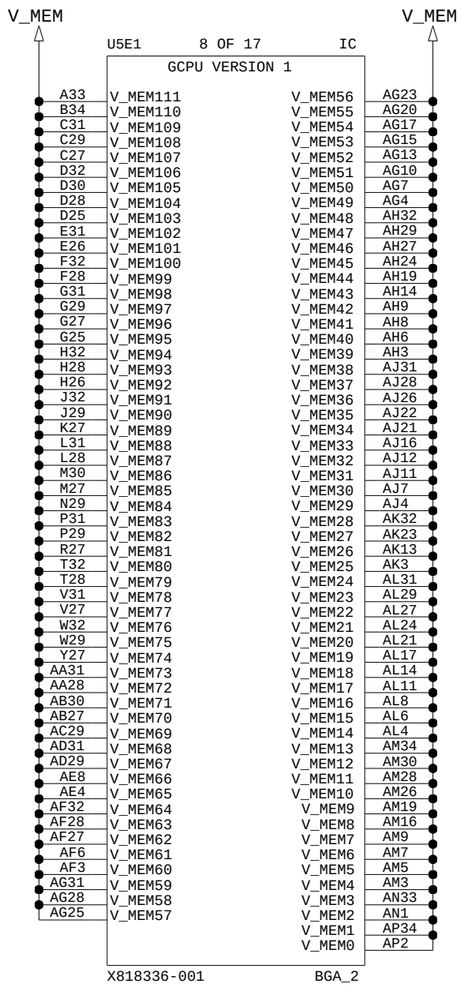
[PAGE_TITLE=GCPU, PLL POWER + FSB POWER]

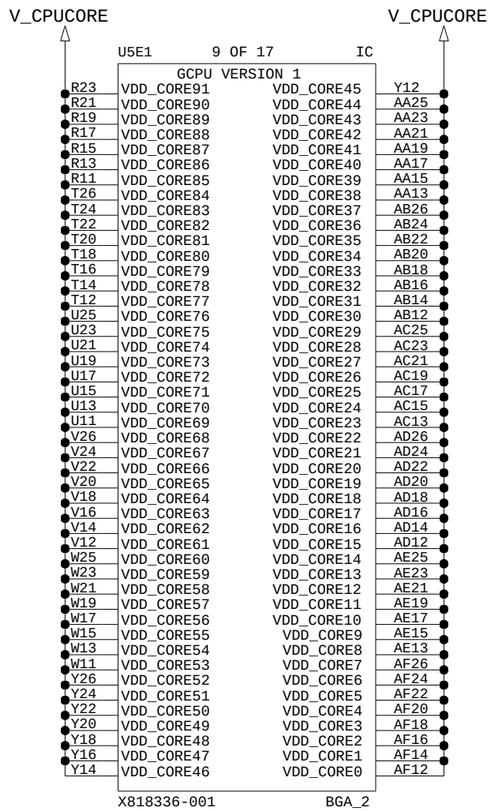
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	6/87	E	1.01

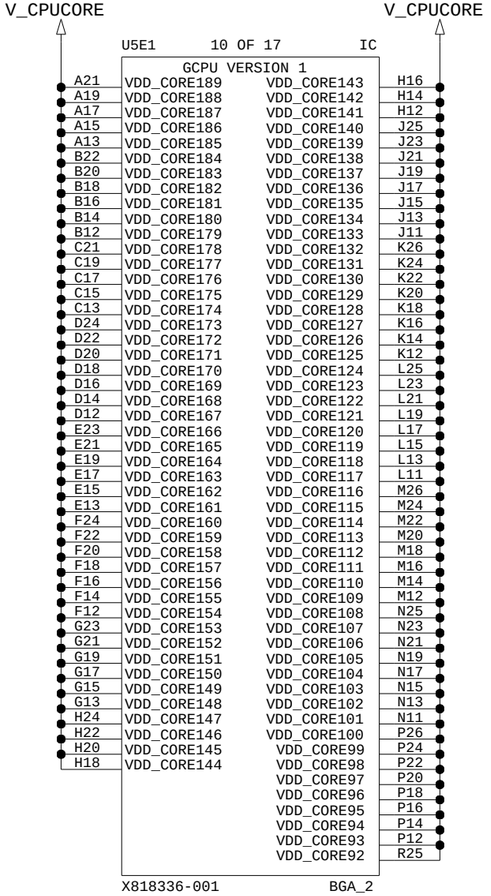
GCPU, POWER











[PAGE_TITLE=GCPU, POWER]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	7/87	E	1.01

GCPU, POWER

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GCPU VERSION 1

Y3	VSS130	VSS65	AF15
AA32	VSS129	VSS64	AF13
AA27	VSS128	VSS63	AF11
AA26	VSS127	VSS62	AF9
AA24	VSS126	VSS61	AF8
AA22	VSS125	VSS60	AF4
AA20	VSS124	VSS59	AG32
AA18	VSS123	VSS58	AG29
AA16	VSS122	VSS57	AG27
AA14	VSS121	VSS56	AG26
AA12	VSS120	VSS55	AG24
AB25	VSS119	VSS54	AG22
AB23	VSS118	VSS53	AG21
AB21	VSS117	VSS52	AG19
AB19	VSS116	VSS51	AG16
AB17	VSS115	VSS50	AG14
AB15	VSS114	VSS49	AG12
AB13	VSS113	VSS48	AG11
AB11	VSS112	VSS47	AG9
AB9	VSS111	VSS46	AG8
AB7	VSS110	VSS45	AG6
AB5	VSS109	VSS44	AG3
AB3	VSS108	VSS43	AH31
AB1	VSS107	VSS42	AH28
AC31	VSS106	VSS41	AH7
AC27	VSS105	VSS40	AH4
AC26	VSS104	VSS39	AJ32
AC24	VSS103	VSS38	AJ29
AC22	VSS102	VSS37	AJ27
AC20	VSS101	VSS36	AJ25
AC18	VSS100	VSS35	AJ20
AC16	VSS99	VSS34	AJ17
AC14	VSS98	VSS33	AJ15
AC12	VSS97	VSS32	AJ10
AD32	VSS96	VSS31	AJ8
AD25	VSS95	VSS30	AJ6
AD23	VSS94	VSS29	AJ3
AD21	VSS93	VSS28	AK31
AD19	VSS92	VSS27	AK18
AD17	VSS91	VSS26	AK4
AD15	VSS90	VSS25	AL32
AD13	VSS89	VSS24	AL30
AD9	VSS88	VSS23	AL28
AD7	VSS87	VSS22	AL26
AD5	VSS86	VSS21	AL22
AD3	VSS85	VSS20	AL19
AE29	VSS84	VSS19	AL16
AE27	VSS83	VSS18	AL12
AE26	VSS82	VSS17	AL9
AE24	VSS81	VSS16	AL7
AE22	VSS80	VSS15	AL5
AE20	VSS79	VSS14	AL3
AE18	VSS78	VSS13	AM33
AE16	VSS77	VSS12	AM31
AE14	VSS76	VSS11	AM29
AE12	VSS75	VSS10	AM27
AE10	VSS74	VSS9	AM24
AE6	VSS73	VSS8	AM21
AE3	VSS72	VSS7	AM14
AF31	VSS71	VSS6	AM11
AF25	VSS70	VSS5	AM8
AF23	VSS69	VSS4	AM6
AF21	VSS68	VSS3	AM4
AF19	VSS67	VSS2	AN34
AF17	VSS66	VSS1	AP33
		VSS0	AP1

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U5E1 12 OF 17 IC

GCPU VERSION 1

K29	VSS260	VSS195	R16
K25	VSS259	VSS194	R14
K23	VSS258	VSS193	R12
K21	VSS257	VSS192	R10
K19	VSS256	VSS191	R8
K17	VSS255	VSS190	T31
K15	VSS254	VSS189	T27
K13	VSS253	VSS188	T25
K11	VSS252	VSS187	T23
K9	VSS251	VSS186	T21
K4	VSS250	VSS185	T19
L32	VSS249	VSS184	T17
L27	VSS248	VSS183	T15
L26	VSS247	VSS182	T13
L24	VSS246	VSS181	T11
L22	VSS245	VSS180	T9
L20	VSS244	VSS179	T7
L18	VSS243	VSS178	T4
L16	VSS242	VSS177	T3
L14	VSS241	VSS176	U30
L12	VSS240	VSS175	U27
L10	VSS239	VSS174	U26
L8	VSS238	VSS173	U24
L3	VSS237	VSS172	U22
M25	VSS236	VSS171	U20
M23	VSS235	VSS170	U18
M21	VSS234	VSS169	U16
M19	VSS233	VSS168	U14
M17	VSS232	VSS167	U12
M15	VSS231	VSS166	U10
M13	VSS230	VSS165	U8
M11	VSS229	VSS164	V29
M9	VSS228	VSS163	V25
M4	VSS227	VSS162	V23
N31	VSS226	VSS161	V21
N27	VSS225	VSS160	V19
N26	VSS224	VSS159	V17
N24	VSS223	VSS158	V15
N22	VSS222	VSS157	V13
N20	VSS221	VSS156	V11
N18	VSS220	VSS155	V9
N16	VSS219	VSS154	V7
N14	VSS218	VSS153	W31
N12	VSS217	VSS152	W26
N10	VSS216	VSS151	W24
N8	VSS215	VSS150	W22
N5	VSS214	VSS149	W20
P32	VSS213	VSS148	W18
P27	VSS212	VSS147	W16
P25	VSS211	VSS146	W14
P23	VSS210	VSS145	W12
P21	VSS209	VSS144	W10
P19	VSS208	VSS143	W8
P17	VSS207	VSS142	W3
P15	VSS206	VSS141	Y29
P13	VSS205	VSS140	Y25
P11	VSS204	VSS139	Y23
P9	VSS203	VSS138	Y21
P6	VSS202	VSS137	Y19
R29	VSS201	VSS136	Y17
R26	VSS200	VSS135	Y15
R24	VSS199	VSS134	Y13
R22	VSS198	VSS133	Y9
R20	VSS197	VSS132	Y7
R18	VSS196	VSS131	Y5

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U5E1 13 OF 17 IC

GCPU VERSION 1

A34	VSS354	VSS318	E24
A22	VSS353	VSS317	E22
A20	VSS352	VSS316	E20
A18	VSS351	VSS315	E18
A16	VSS350	VSS314	E16
A14	VSS349	VSS313	E14
A12	VSS348	VSS312	E12
A10	VSS347	VSS311	E10
B33	VSS346	VSS310	E6
B21	VSS345	VSS309	F31
B19	VSS344	VSS308	F29
B17	VSS343	VSS307	F27
B15	VSS342	VSS306	F23
B13	VSS341	VSS305	F21
B11	VSS340	VSS304	F19
B7	VSS339	VSS303	F17
C28	VSS338	VSS302	F15
C25	VSS337	VSS301	F13
C22	VSS336	VSS300	F11
C20	VSS335	VSS299	F9
C18	VSS334	VSS298	F4
C16	VSS333	VSS297	G32
C14	VSS332	VSS296	G28
C12	VSS331	VSS295	G24
C10	VSS330	VSS294	G22
D31	VSS329	VSS293	G20
D29	VSS328	VSS292	G18
D27	VSS327	VSS291	G16
D23	VSS326	VSS290	G14
D21	VSS325	VSS289	G12
D19	VSS324	VSS288	G10
D17	VSS323	VSS287	G8
D15	VSS322	VSS286	G3
D13	VSS321	VSS285	H31
D11	VSS320	VSS284	H29
E32	VSS319	VSS283	H27
		VSS282	H23
		VSS281	H21
		VSS280	H19
		VSS279	H17
		VSS278	H15
		VSS277	H13
		VSS276	H11
		VSS275	H9
		VSS274	H7
		VSS273	J31
		VSS272	J27
		VSS271	J24
		VSS270	J22
		VSS269	J20
		VSS268	J18
		VSS267	J16
		VSS266	J14
		VSS265	J12
		VSS264	J10
		VSS263	J8
		VSS261	J3

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[PAGE_TITLE=GCPU, POWER]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	8/87	E	1.01

GCPU, DECOUPLING

V_CPUCORE

C6R4 4.7 UF 10% 6.3 V X5R 603
C5D13 4.7 UF 10% 6.3 V X5R 603
C5R8 4.7 UF 10% 6.3 V X5R 603
C5R9 4.7 UF 10% 6.3 V X5R 603
C5R15 4.7 UF 10% 6.3 V X5R 603
C5D14 4.7 UF 10% 6.3 V X5R 603
C6D3 4.7 UF 10% 6.3 V X5R 603
C5D7 4.7 UF 10% 6.3 V X5R 603
C6R3 4.7 UF 10% 6.3 V X5R 603
C5D3 4.7 UF 10% 6.3 V X5R 603
C5R7 4.7 UF 10% 6.3 V X5R 603
C5D6 4.7 UF 10% 6.3 V X5R 603
C5R10 4.7 UF 10% 6.3 V X5R 603
C5D8 4.7 UF 10% 6.3 V X5R 603
C6R6 4.7 UF 10% 6.3 V X5R 603
C5D5 4.7 UF 10% 6.3 V X5R 603
C5D12 4.7 UF 10% 6.3 V X5R 603
C5R6 4.7 UF 10% 6.3 V X5R 603
C6D4 4.7 UF 10% 6.3 V X5R 603
C5D9 4.7 UF 10% 6.3 V X5R 603
C6R2 4.7 UF 10% 6.3 V X5R 603
C5R5 4.7 UF 10% 6.3 V X5R 603
C6R1 4.7 UF 10% 6.3 V X5R 603
C5R18 4.7 UF 10% 6.3 V X5R 603
C5R12 4.7 UF 10% 6.3 V X5R 603
C5D2 4.7 UF 10% 6.3 V X5R 603
C5R3 4.7 UF 10% 6.3 V X5R 603
C5D10 4.7 UF 10% 6.3 V X5R 603
C6D5 4.7 UF 10% 6.3 V X5R 603
C5R16 4.7 UF 10% 6.3 V X5R 603
C6R7 4.7 UF 10% 6.3 V X5R 603
C5D11 4.7 UF 10% 6.3 V X5R 603
C6D1 4.7 UF 10% 6.3 V X5R 603
C6D2 4.7 UF 10% 6.3 V X5R 603
C6D6 4.7 UF 10% 6.3 V X5R 603
C5T33 4.7 UF 10% 6.3 V X5R 603
C6R5 4.7 UF 10% 6.3 V X5R 603
C5R13 4.7 UF 10% 6.3 V X5R 603
C5R2 4.7 UF 10% 6.3 V X5R 603
C6T22 4.7 UF 10% 6.3 V X5R 603
C6T23 4.7 UF 10% 6.3 V X5R 603

V_CPUEDRAM

C5T26 0.1 UF 10% 6.3 V X5R 402
C5E6 4.7 UF 10% 6.3 V X5R 603
C5T32 0.1 UF 10% 6.3 V X5R 402
C5E5 4.7 UF 10% 6.3 V X5R 603
C5T24 0.1 UF 10% 6.3 V X5R 402
C5T35 4.7 UF 10% 6.3 V X5R 603
C5T31 0.1 UF 10% 6.3 V X5R 402
C5E7 4.7 UF 10% 6.3 V X5R 603
C5T27 0.1 UF 10% 6.3 V X5R 402
C5T34 4.7 UF 10% 6.3 V X5R 603
C5T22 0.1 UF 10% 6.3 V X5R 402
C5T43 4.7 UF 10% 6.3 V X5R 603
C5T23 0.1 UF 10% 6.3 V X5R 402
C5E8 4.7 UF 10% 6.3 V X5R 603
C5T20 0.1 UF 10% 6.3 V X5R 402
C5E9 4.7 UF 10% 6.3 V X5R 603
C5T25 0.1 UF 10% 6.3 V X5R 402
C4T3 4.7 UF 10% 6.3 V X5R 603
C5T21 0.1 UF 10% 6.3 V X5R 402
C4T4 4.7 UF 10% 6.3 V X5R 603

V_CPUVCS

C5R35 0.1 UF 10% 6.3 V X5R 402
C5D1 4.7 UF 10% 6.3 V X5R 603
C5R58 0.1 UF 10% 6.3 V X5R 402
C5R4 4.7 UF 10% 6.3 V X5R 603
C5R43 0.1 UF 10% 6.3 V X5R 402
C5D4 4.7 UF 10% 6.3 V X5R 603
C5T7 0.1 UF 10% 6.3 V X5R 402
C5R1 4.7 UF 10% 6.3 V X5R 603
C5R50 0.1 UF 10% 6.3 V X5R 402
C5T1 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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Thu Feb 17 10:12:27 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	9/87	E	1.01

GCPU, DECOUPLING

V_CPUCORE

C5T12	C5R26	C5T17	C5T10	C6R36
C5R33	C6R25	C6T11	C5T8	C5R63
C5R39	C5R60	C6R42	C6R45	C5R28
C5R40	C5R61	C5R37	C5R49	C5R59
C6T7	C6T20	C6R37	C6R33	C5R27
C5R38	C5R32	C5R57	C6T8	C5R62
C6T12	C6T6	C5R64	C6R15	C5R55
C6R31	C6R28	C5R46	C6R21	C5R51
C6R38	C5R36	C5R45	C6R20	C6R18
C6R43	C5T11	C6T14	C6R44	C6R17

Each: 1 — 2, 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	10/87	E	1.01

GCPU, DECOUPLING

V_CPUCORE

C5R25 1 2 0.1 UF 10% 6.3 V X5R 402
C6R8 1 2 0.1 UF 10% 6.3 V X5R 402
C6R39 1 2 0.1 UF 10% 6.3 V X5R 402
C5R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6T5 1 2 0.1 UF 10% 6.3 V X5R 402
C5T14 1 2 0.1 UF 10% 6.3 V X5R 402
C6T15 1 2 0.1 UF 10% 6.3 V X5R 402
C6R34 1 2 0.1 UF 10% 6.3 V X5R 402
C6T3 1 2 0.1 UF 10% 6.3 V X5R 402
C5R52 1 2 0.1 UF 10% 6.3 V X5R 402
C5R21 1 2 0.1 UF 10% 6.3 V X5R 402
C6T9 1 2 0.1 UF 10% 6.3 V X5R 402
C5T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R35 1 2 0.1 UF 10% 6.3 V X5R 402
C5T15 1 2 0.1 UF 10% 6.3 V X5R 402
C5T16 1 2 0.1 UF 10% 6.3 V X5R 402
C5T3 1 2 0.1 UF 10% 6.3 V X5R 402
C6T18 1 2 0.1 UF 10% 6.3 V X5R 402
C5R53 1 2 0.1 UF 10% 6.3 V X5R 402
C6R22 1 2 0.1 UF 10% 6.3 V X5R 402
C5T28 1 2 0.1 UF 10% 6.3 V X5R 402
C6T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R13 1 2 0.1 UF 10% 6.3 V X5R 402
C6R9 1 2 0.1 UF 10% 6.3 V X5R 402
C5T30 1 2 0.1 UF 10% 6.3 V X5R 402
C5R44 1 2 0.1 UF 10% 6.3 V X5R 402
C5R41 1 2 0.1 UF 10% 6.3 V X5R 402
C6T25 1 2 0.1 UF 10% 6.3 V X5R 402
C5R34 1 2 0.1 UF 10% 6.3 V X5R 402
C6R10 1 2 0.1 UF 10% 6.3 V X5R 402
C5T29 1 2 0.1 UF 10% 6.3 V X5R 402
C5R47 1 2 0.1 UF 10% 6.3 V X5R 402
C6R24 1 2 0.1 UF 10% 6.3 V X5R 402
C6R12 1 2 0.1 UF 10% 6.3 V X5R 402
C6R14 1 2 0.1 UF 10% 6.3 V X5R 402
C5R20 1 2 0.1 UF 10% 6.3 V X5R 402
C5R24 1 2 0.1 UF 10% 6.3 V X5R 402
C5R48 1 2 0.1 UF 10% 6.3 V X5R 402
C6T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T5 1 2 0.1 UF 10% 6.3 V X5R 402
C5R19 1 2 0.1 UF 10% 6.3 V X5R 402
C5R56 1 2 0.1 UF 10% 6.3 V X5R 402
C6R26 1 2 0.1 UF 10% 6.3 V X5R 402
C6T16 1 2 0.1 UF 10% 6.3 V X5R 402
C6T17 1 2 0.1 UF 10% 6.3 V X5R 402
C6T13 1 2 0.1 UF 10% 6.3 V X5R 402
C5R22 1 2 0.1 UF 10% 6.3 V X5R 402
C6T4 1 2 0.1 UF 10% 6.3 V X5R 402
C6R32 1 2 0.1 UF 10% 6.3 V X5R 402
C5T18 1 2 0.1 UF 10% 6.3 V X5R 402
C6R40 1 2 0.1 UF 10% 6.3 V X5R 402
C6T24 1 2 0.1 UF 10% 6.3 V X5R 402
C5R23 1 2 0.1 UF 10% 6.3 V X5R 402
C5R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6R41 1 2 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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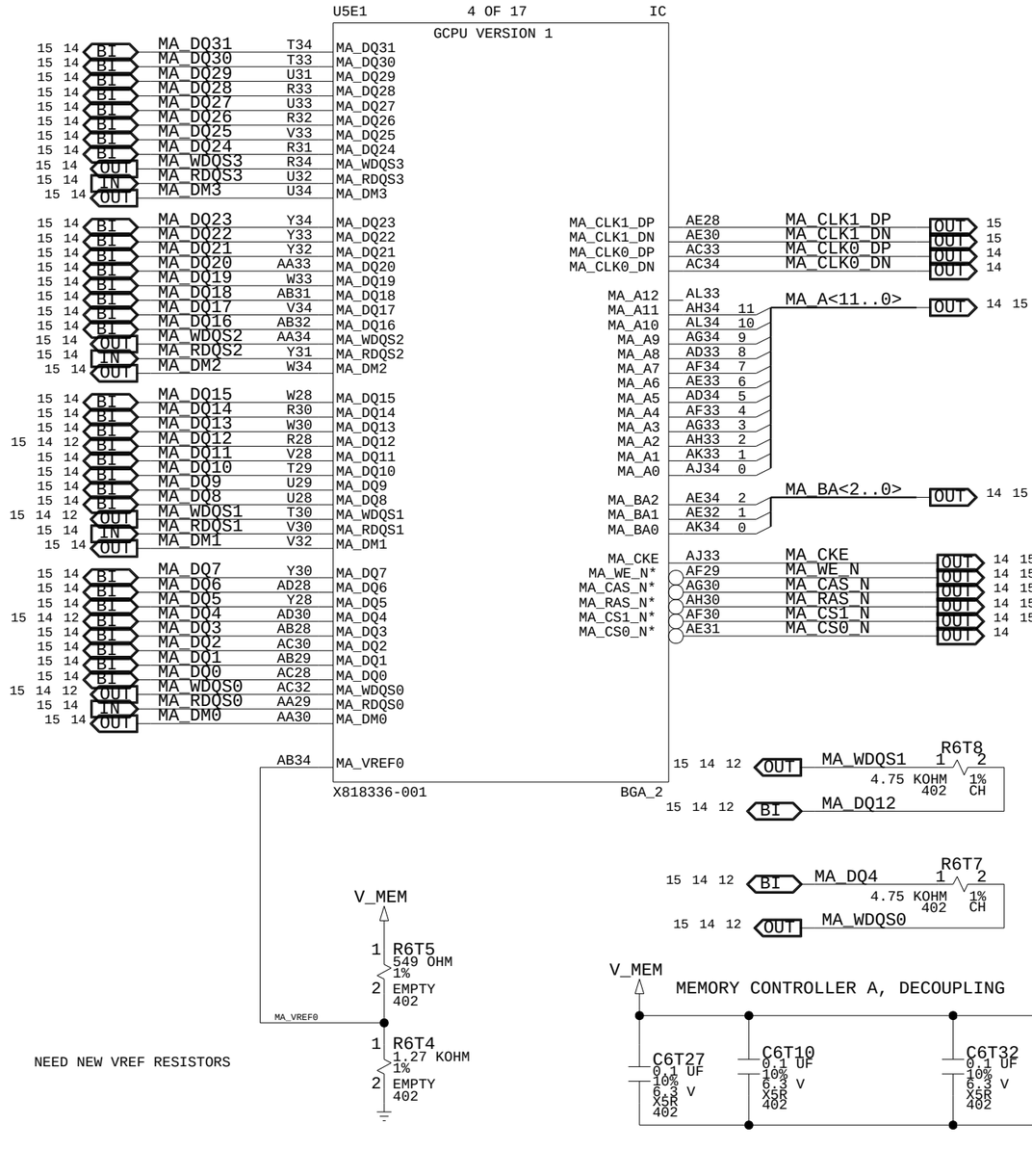
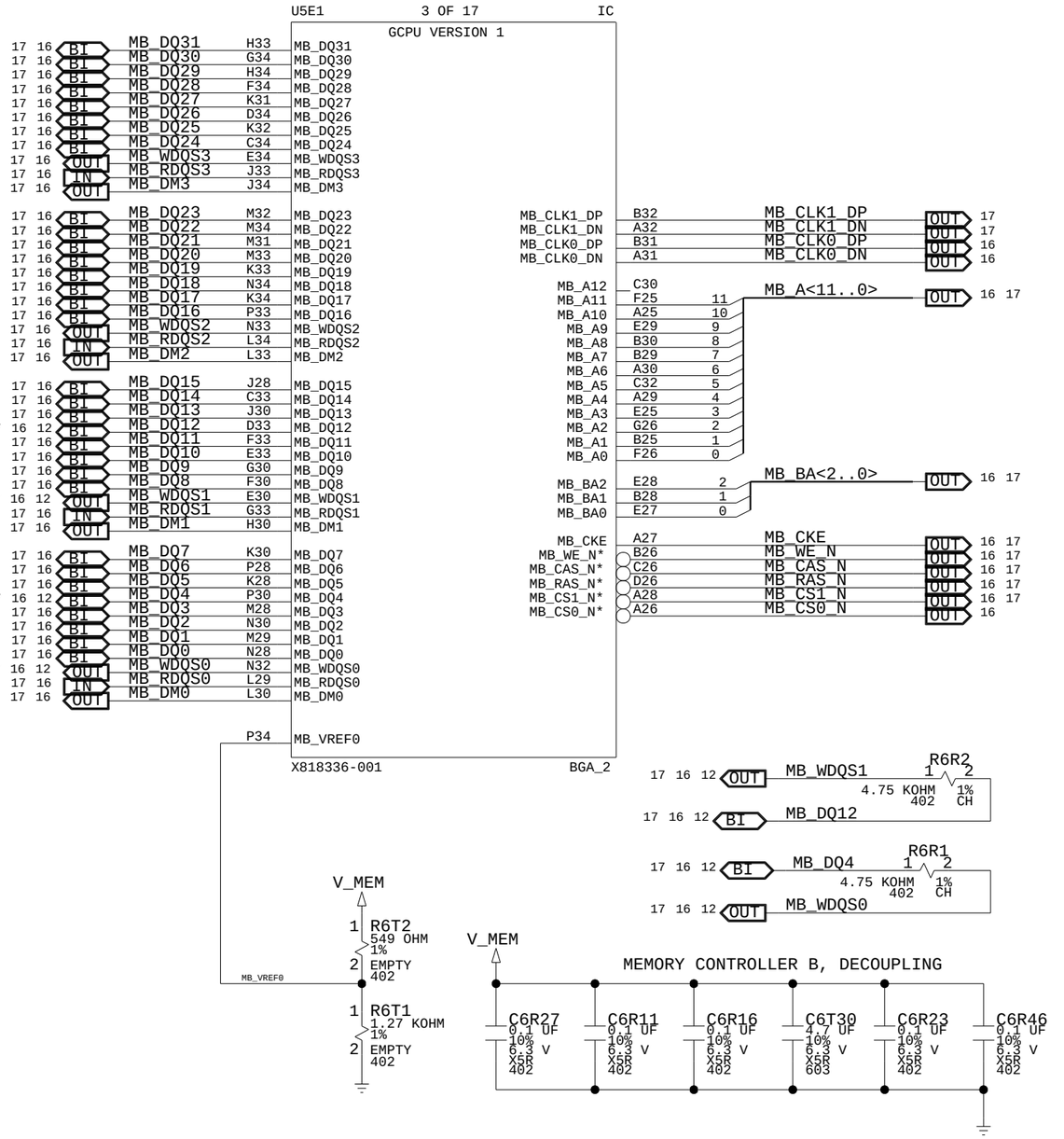
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	11/87	E	1.01

GPU, MEMORY CONTROLLER 0 PARTITION A & B





TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	12/87	E	1.01

GPU, MEMORY CONTROLLER 1 PARTITION C & D

U5E1 2 OF 17 IC

GCPU VERSION 1

MC_DQ31 AP15 MC_DQ31
MC_DQ30 AM15 MC_DQ30
MC_DQ29 AN15 MC_DQ29
MC_DQ28 AL15 MC_DQ28
MC_DQ27 AL13 MC_DQ27
MC_DQ26 AN16 MC_DQ26
MC_DQ25 AM13 MC_DQ25
MC_DQ24 AP17 MC_DQ24
MC_WDQS3 AP16 MC_WDQS3
MC_RDQS3 AN14 MC_RDQS3
MC_DM3 AP14 MC_DM3

MC_DQ23 AP11 MC_DQ23
MC_DQ22 AL10 MC_DQ22
MC_DQ21 AN11 MC_DQ21
MC_DQ20 AM10 MC_DQ20
MC_DQ19 AN13 MC_DQ19
MC_DQ18 AN10 MC_DQ18
MC_DQ17 AP13 MC_DQ17
MC_DQ16 AN9 MC_DQ16
MC_WDQS2 AP10 MC_WDQS2
MC_RDQS2 AP12 MC_RDQS2
MC_DM2 AN12 MC_DM2

MC_DQ15 AJ9 MC_DQ15
MC_DQ14 AJ13 MC_DQ14
MC_DQ13 AK9 MC_DQ13
MC_DQ12 AH13 MC_DQ12
MC_DQ11 AK11 MC_DQ11
MC_DQ10 AK12 MC_DQ10
MC_DQ9 AH11 MC_DQ9
MC_DQ8 AM12 MC_DQ8
MC_WDQS1 AH12 MC_WDQS1
MC_RDQS1 AK10 MC_RDQS1
MC_DM1 AH10 MC_DM1

MC_DQ7 AN8 MC_DQ7
MC_DQ6 AN2 MC_DQ6
MC_DQ5 AK8 MC_DQ5
MC_DQ4 AN3 MC_DQ4
MC_DQ3 AN6 MC_DQ3
MC_DQ2 AK5 MC_DQ2
MC_DQ1 AK6 MC_DQ1
MC_DQ0 AN5 MC_DQ0
MC_WDQS0 AN4 MC_WDQS0
MC_RDQS0 AK7 MC_RDQS0
MC_DM0 AN7 MC_DM0

AE5 MC_VREF0

X818336-001 BGA_2

MC_CLK1_DP AP9 MC_CLK1_DP → OUT 19
MC_CLK1_DN AP8 MC_CLK1_DN → OUT 19
MC_CLK0_DP AP6 MC_CLK0_DP → OUT 18
MC_CLK0_DN AP5 MC_CLK0_DN → OUT 18

MC_A12 AE1
MC_A11 AH1 11
MC_A10 AE2 10
MC_A9 AJ2 9
MC_A8 AP4 8
MC_A7 AK1 7
MC_A6 AL1 6
MC_A5 AP3 5
MC_A4 AK2 4
MC_A3 AJ1 3
MC_A2 AH2 2
MC_A1 AF1 1
MC_A0 AG2 0
→ MC_A<11..0> OUT 18 19

MC_BA2 AL2 2
MC_BA1 AM1 1
MC_BA0 AF2 0
→ MC_BA<2..0> OUT 18 19

MC_CKE AG1 → MC_CKE OUT 18 19
MC_WE_N* AH5 → MC_WE_N OUT 18 19
MC_CAS_N* AG5 → MC_CAS_N OUT 18 19
MC_RAS_N* AF5 → MC_RAS_N OUT 18 19
MC_CS1_N* AJ5 → MC_CS1_N OUT 18 19
MC_CS0_N* AM2 → MC_CS0_N OUT 18

19 18 13 OUT MC_WDQS1 R5T7 1 2 4.75 KOHM 402 1% CH
19 18 13 BI MC_DQ12

19 18 13 BI MC_DQ4 R5T6 1 2 4.75 KOHM 402 1% CH
19 18 13 OUT MC_WDQS0

V_MEM
R5T2 549 OHM 1% EMPTY 402
MC_VREF0
R5T3 1.27 KOHM 1% EMPTY 402

NEED TO VREF RESISTOR VALUES

V_MEM
MEMORY CONTROLLER C, DECOUPLING
C5U2 4.7 UF 10% 6.3 V X5R 603
C5T37 C5T41 C6T28 C5T49 C5T50 C5T46 C6T33 C5T47
0.1 UF 10% 6.3 V X5R 402

TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

GPU MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

U5E1 1 OF 17 IC

GCPU VERSION 1

MD_DQ31 AM23 MD_DQ31
MD_DQ30 AL23 MD_DQ30
MD_DQ29 AP23 MD_DQ29
MD_DQ28 AP24 MD_DQ28
MD_DQ27 AP22 MD_DQ27
MD_DQ26 AN25 MD_DQ26
MD_DQ25 AN21 MD_DQ25
MD_DQ24 AP25 MD_DQ24
MD_WDQS3 AN24 MD_WDQS3
MD_RDQS3 AN23 MD_RDQS3
MD_DM3 AN22 MD_DM3

MD_DQ23 AN19 MD_DQ23
MD_DQ22 AP19 MD_DQ22
MD_DQ21 AN20 MD_DQ21
MD_DQ20 AL18 MD_DQ20
MD_DQ19 AL20 MD_DQ19
MD_DQ18 AP18 MD_DQ18
MD_DQ17 AP21 MD_DQ17
MD_DQ16 AN18 MD_DQ16
MD_WDQS2 AM18 MD_WDQS2
MD_RDQS2 AP20 MD_RDQS2
MD_DM2 AM20 MD_DM2

MD_DQ15 AJ19 MD_DQ15
MD_DQ14 AH23 MD_DQ14
MD_DQ13 AK19 MD_DQ13
MD_DQ12 AJ23 MD_DQ12
MD_DQ11 AK21 MD_DQ11
MD_DQ10 AK22 MD_DQ10
MD_DQ9 AH21 MD_DQ9
MD_DQ8 AM22 MD_DQ8
MD_WDQS1 AH22 MD_WDQS1
MD_RDQS1 AK20 MD_RDQS1
MD_DM1 AH20 MD_DM1

MD_DQ7 AH18 MD_DQ7
MD_DQ6 AJ14 MD_DQ6
MD_DQ5 AJ18 MD_DQ5
MD_DQ4 AK14 MD_DQ4
MD_DQ3 AM17 MD_DQ3
MD_DQ2 AK15 MD_DQ2
MD_DQ1 AK16 MD_DQ1
MD_DQ0 AH16 MD_DQ0
MD_WDQS0 AH15 MD_WDQS0
MD_RDQS0 AK17 MD_RDQS0
MD_DM0 AH17 MD_DM0

AN17 MD_VREF0

X818336-001 BGA_2

MD_CLK1_DP AJ24 MD_CLK1_DP → OUT 21
MD_CLK1_DN AK24 MD_CLK1_DN → OUT 21
MD_CLK0_DP AL25 MD_CLK0_DP → OUT 20
MD_CLK0_DN AM25 MD_CLK0_DN → OUT 20

MD_A12 AK30
MD_A11 AN31 11
MD_A10 AN32 10
MD_A9 AK26 9
MD_A8 AK25 8
MD_A7 AN26 7
MD_A6 AH26 6
MD_A5 AH25 5
MD_A4 AN27 4
MD_A3 AP32 3
MD_A2 AN29 2
MD_A1 AM32 1
MD_A0 AN30 0
→ MD_A<11..0> OUT 20 21

MD_BA2 AK27 2
MD_BA1 AN28 1
MD_BA0 AK29 0
→ MD_BA<2..0> OUT 20 21

MD_CKE AP30 → MD_CKE OUT 20 21
MD_WE_N* AP28 → MD_WE_N OUT 20 21
MD_CAS_N* AP29 → MD_CAS_N OUT 20 21
MD_RAS_N* AP31 → MD_RAS_N OUT 20 21
MD_CS1_N* AK28 → MD_CS1_N OUT 20 21
MD_CS0_N* AP27 → MD_CS0_N OUT 20

21 20 13 OUT MD_WDQS1 R6T9 1 2 4.75 KOHM 402 1% CH
21 20 13 BI MD_DQ12

V_MEM
R5T5 549 OHM 1% EMPTY 402
MD_VREF0
R5T4 1.27 KOHM 1% EMPTY 402

V_MEM
MEMORY CONTROLLER D, DECOUPLING
C5T48 C5T39 C6T31 C5T38 C6T26 C5T42 C5T45 C5T44
0.1 UF 10% 6.3 V X5R 402

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

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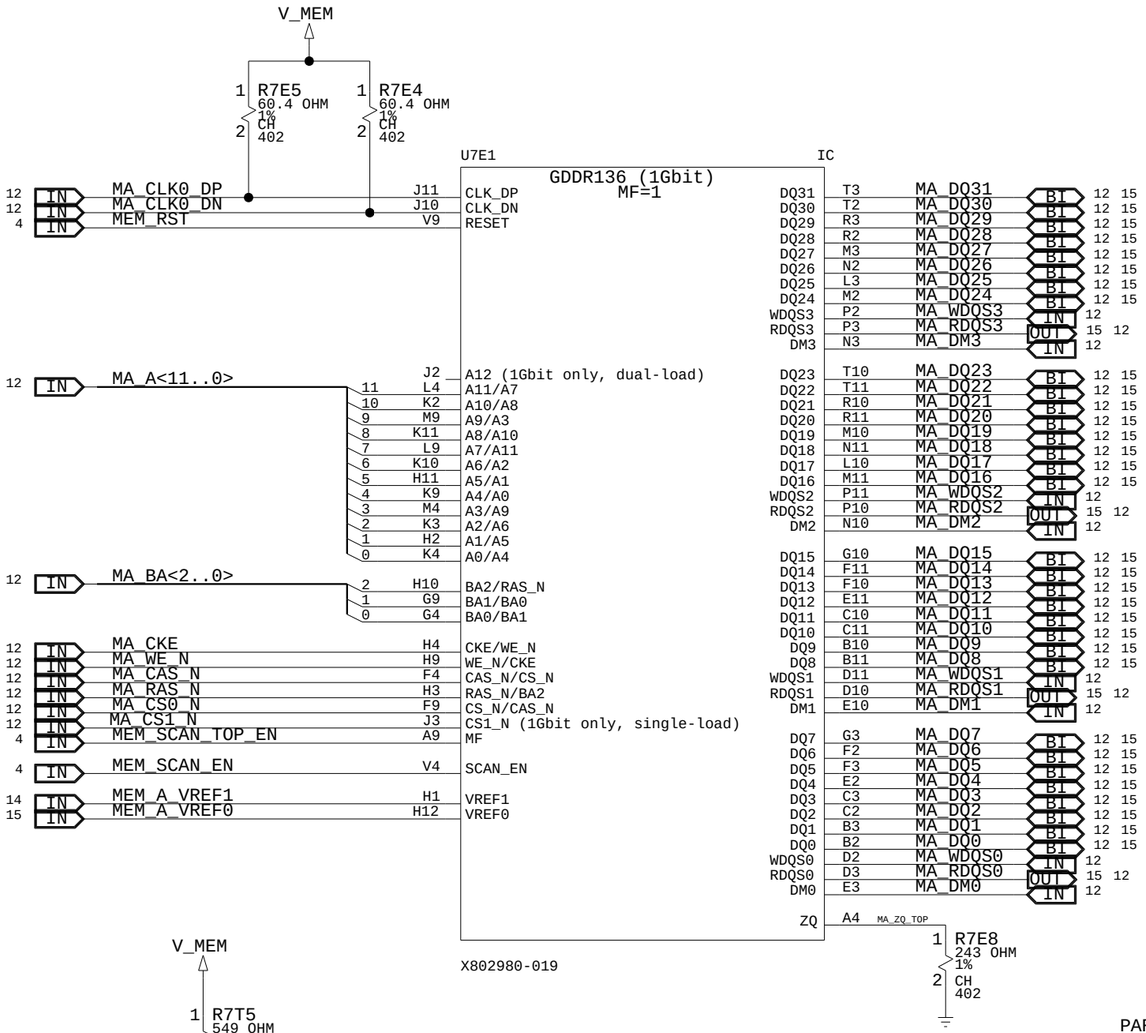
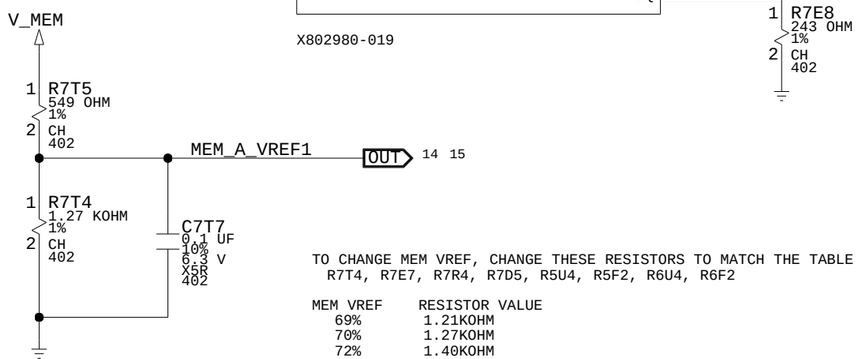
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	13/87	E	1.01

MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

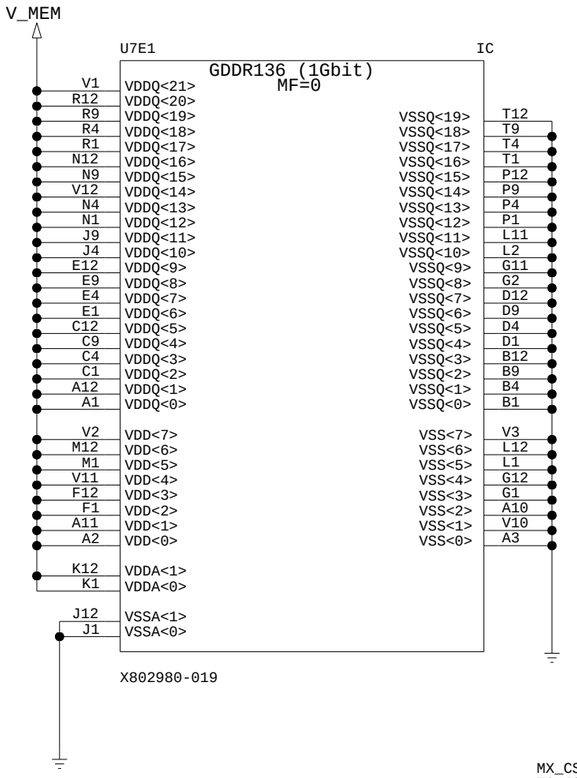




TO CHANGE MEM VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R7T4, R7E7, R7R4, R7D5, R5U4, R5F2, R6U4, R6F2

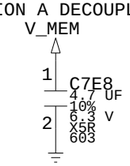
MEM VREF	RESISTOR VALUE
69%	1.21KOHM
70%	1.27KOHM
72%	1.40KOHM

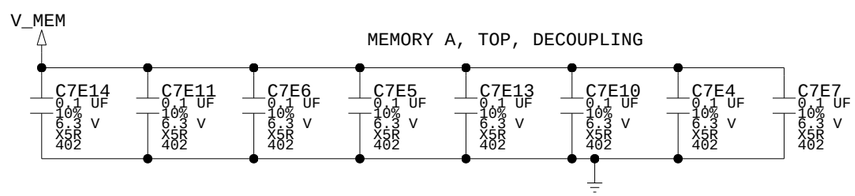
THESE ARE THE MEM VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.



MX_CS1_N CONNECTED TO J3 TO SUPPORT 1G RAM CONFIGS.

PARTITION A DECOUPLING





[PAGE_TITLE=MEMORY PARTITION A, TOP]

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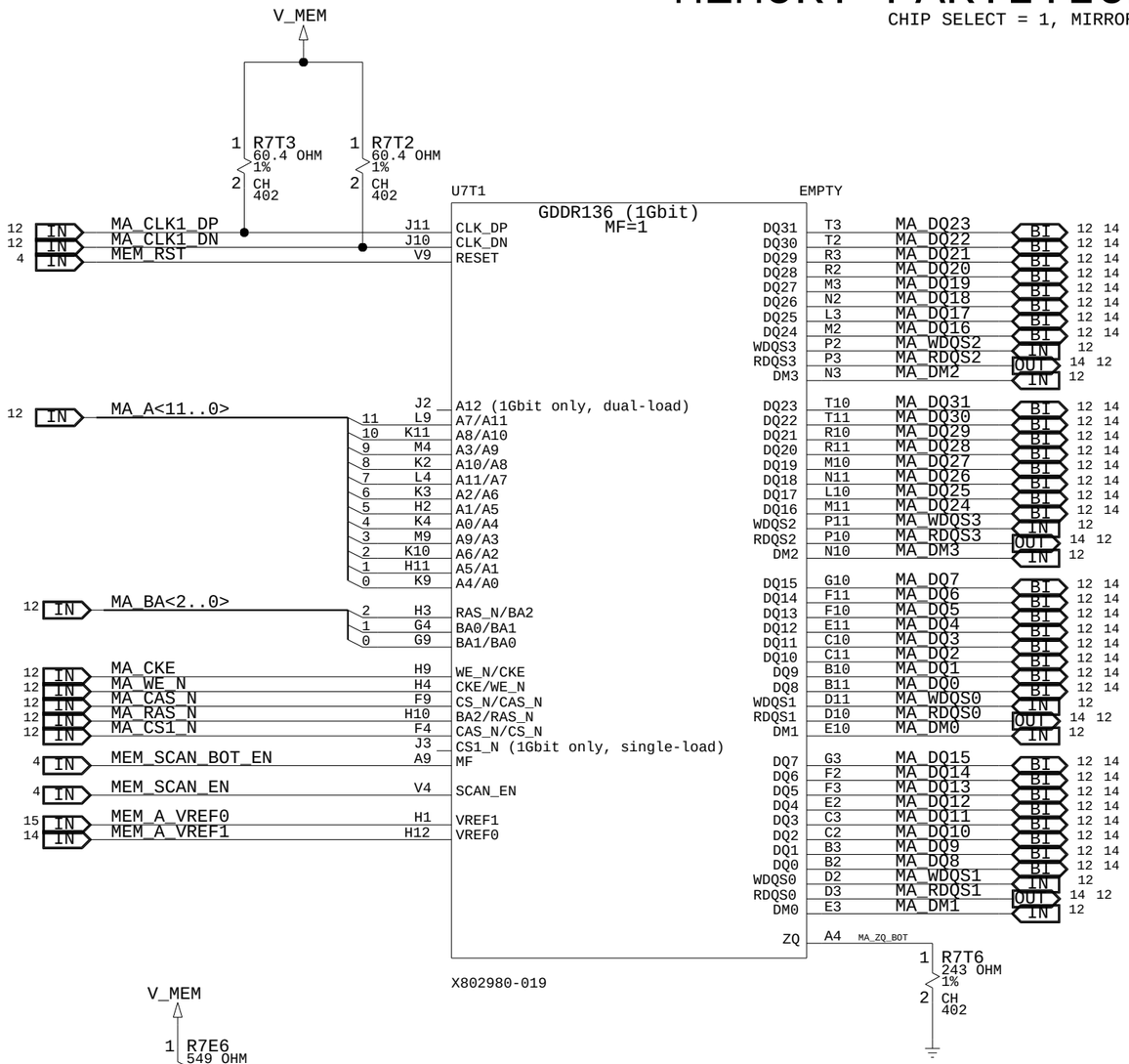
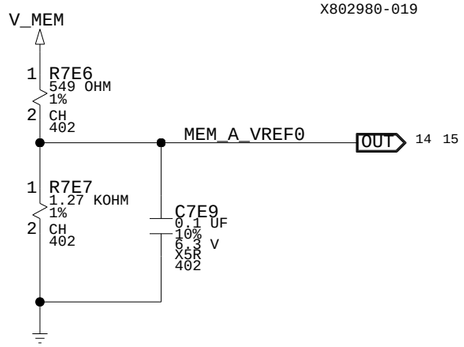
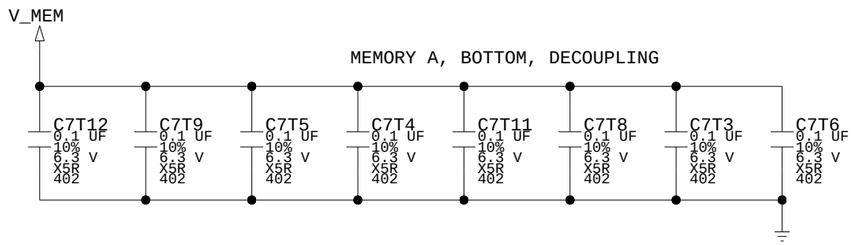
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	14/87	E	1.01

MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1







[PAGE_TITLE=MEMORY PARTITION A, BOTTOM]

DRAWING
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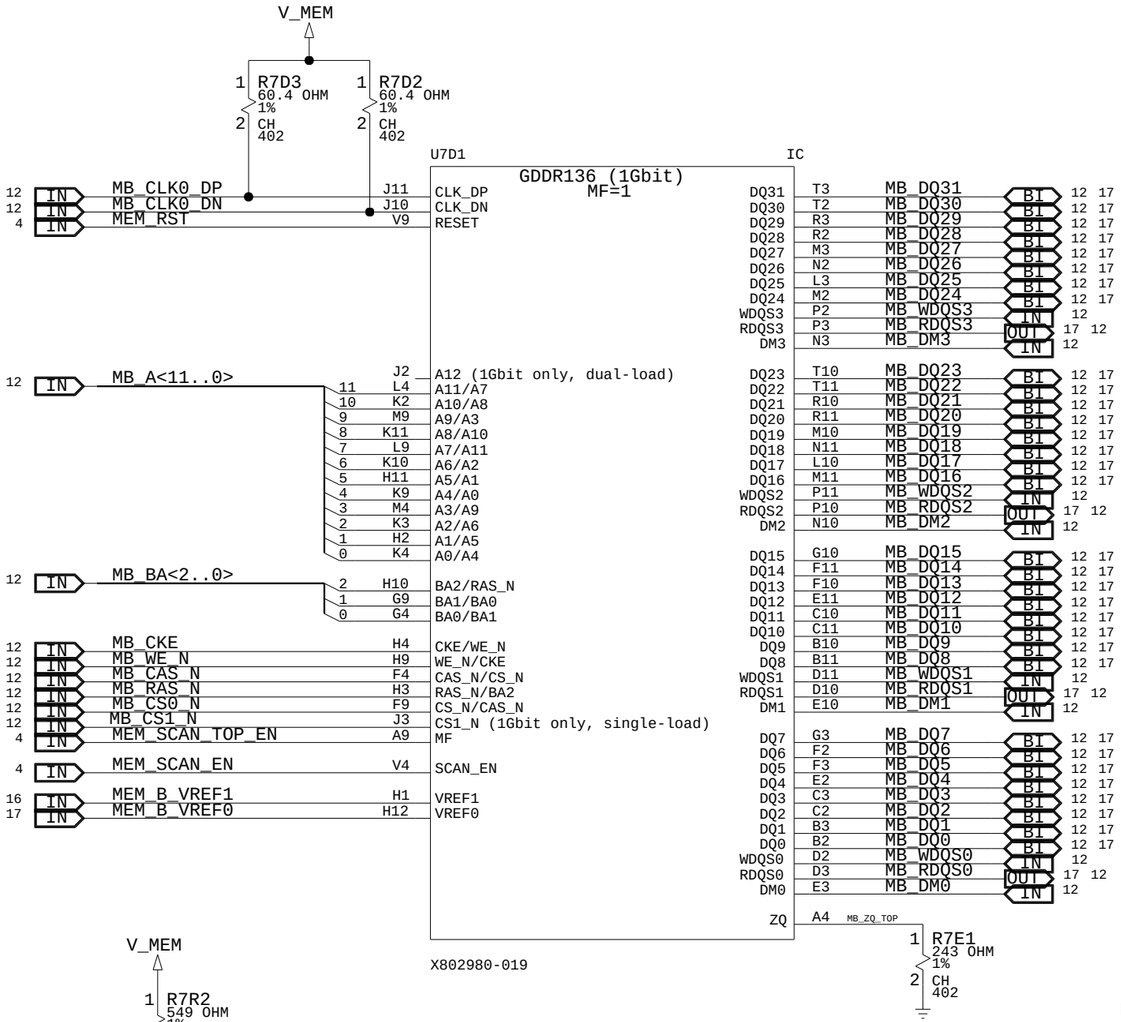
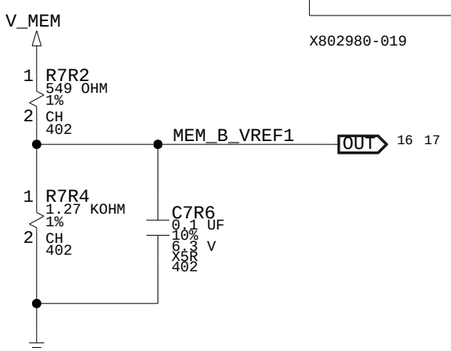
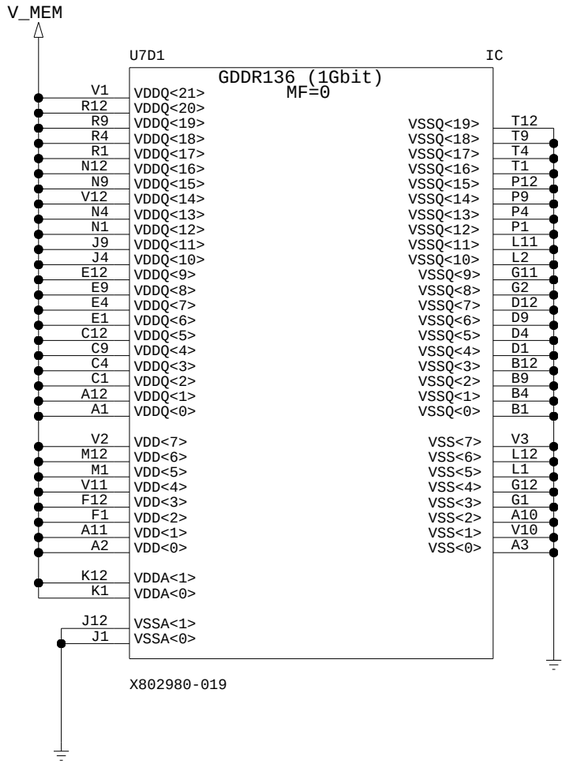
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	15/87	E	1.01

MEMORY PARTITION B, TOP

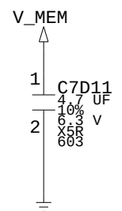
CHIP SELECT = 0, MIRROR FUNCTION = 0

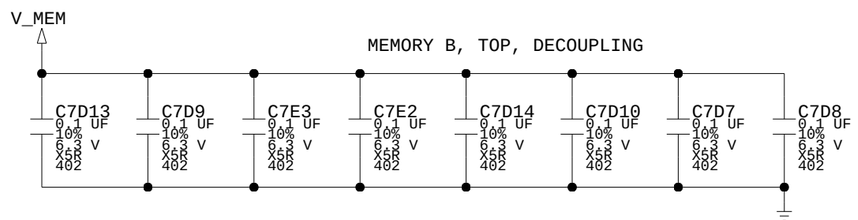






PARTITION B DECOUPLING





[PAGE_TITLE=MEMORY PARITION B, TOP]

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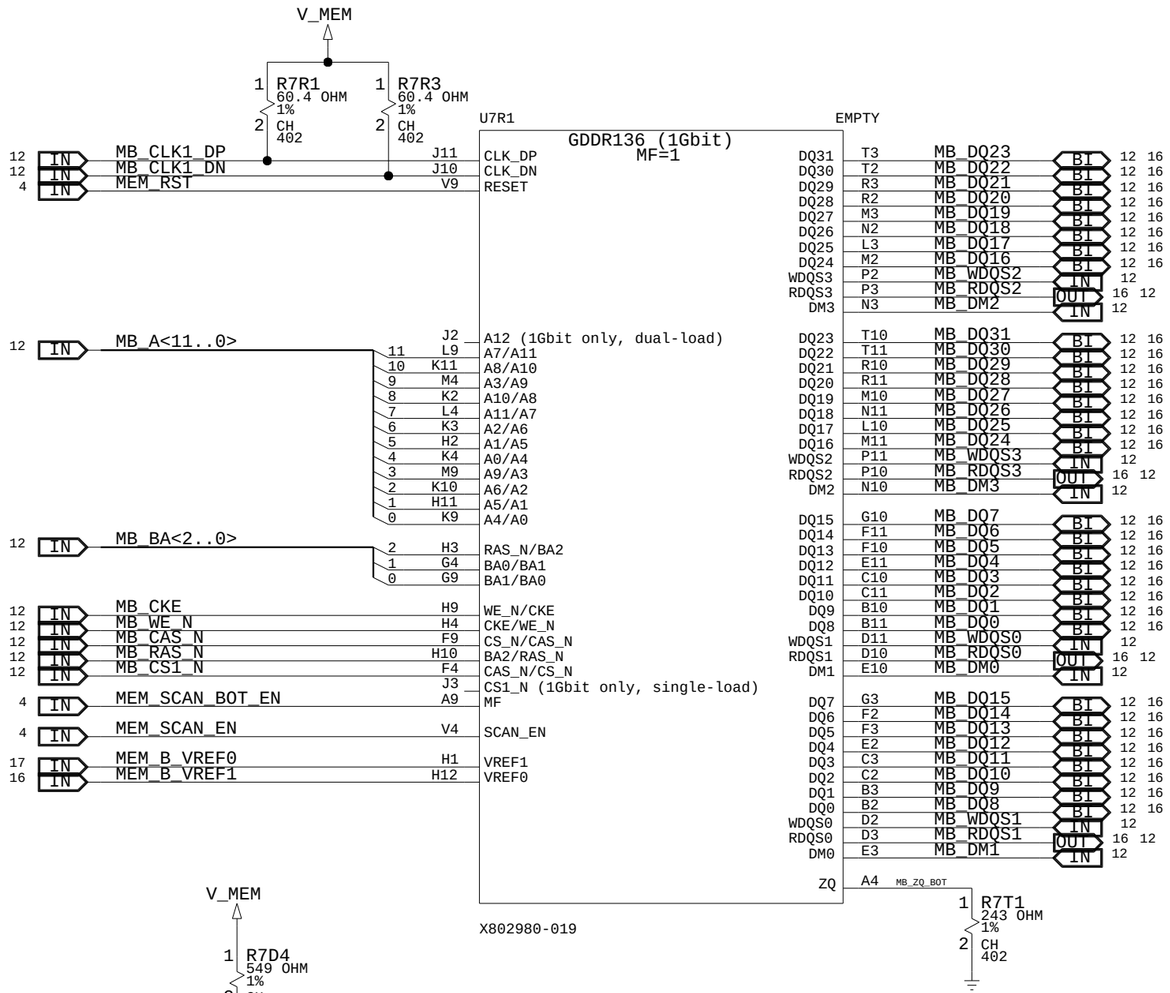
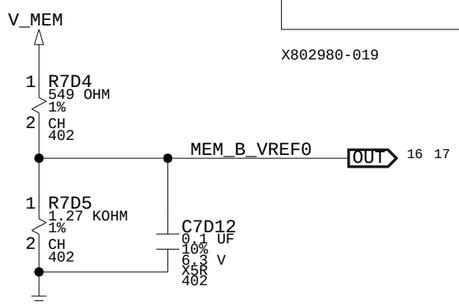
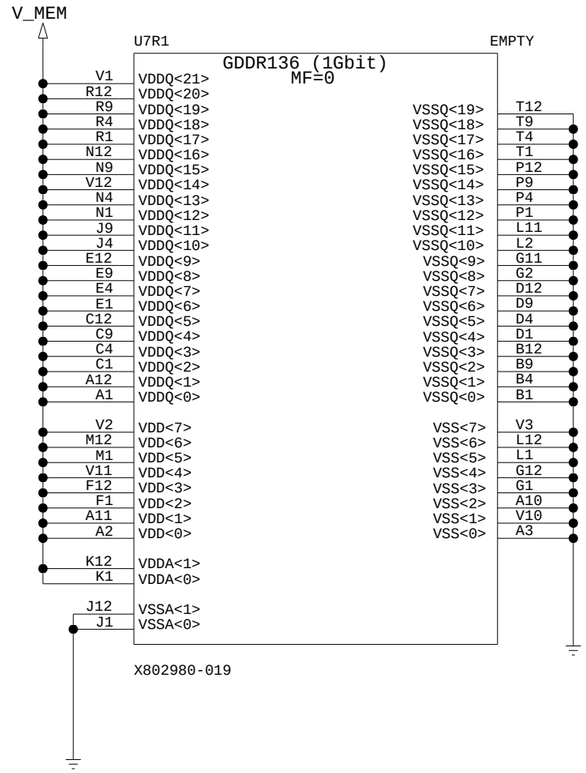
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	16/87	E	1.01

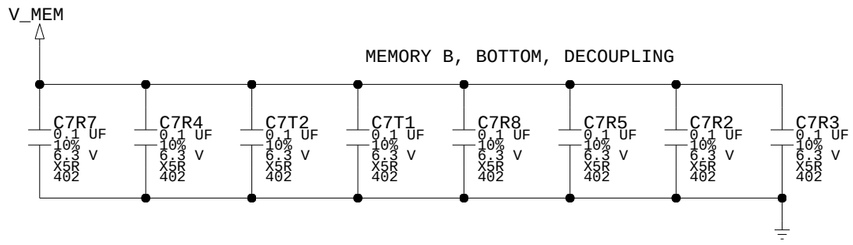
MEMORY PARTITION B, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1









[PAGE_TITLE=MEMORY PARITION B, BOTTOM]

DRAWING
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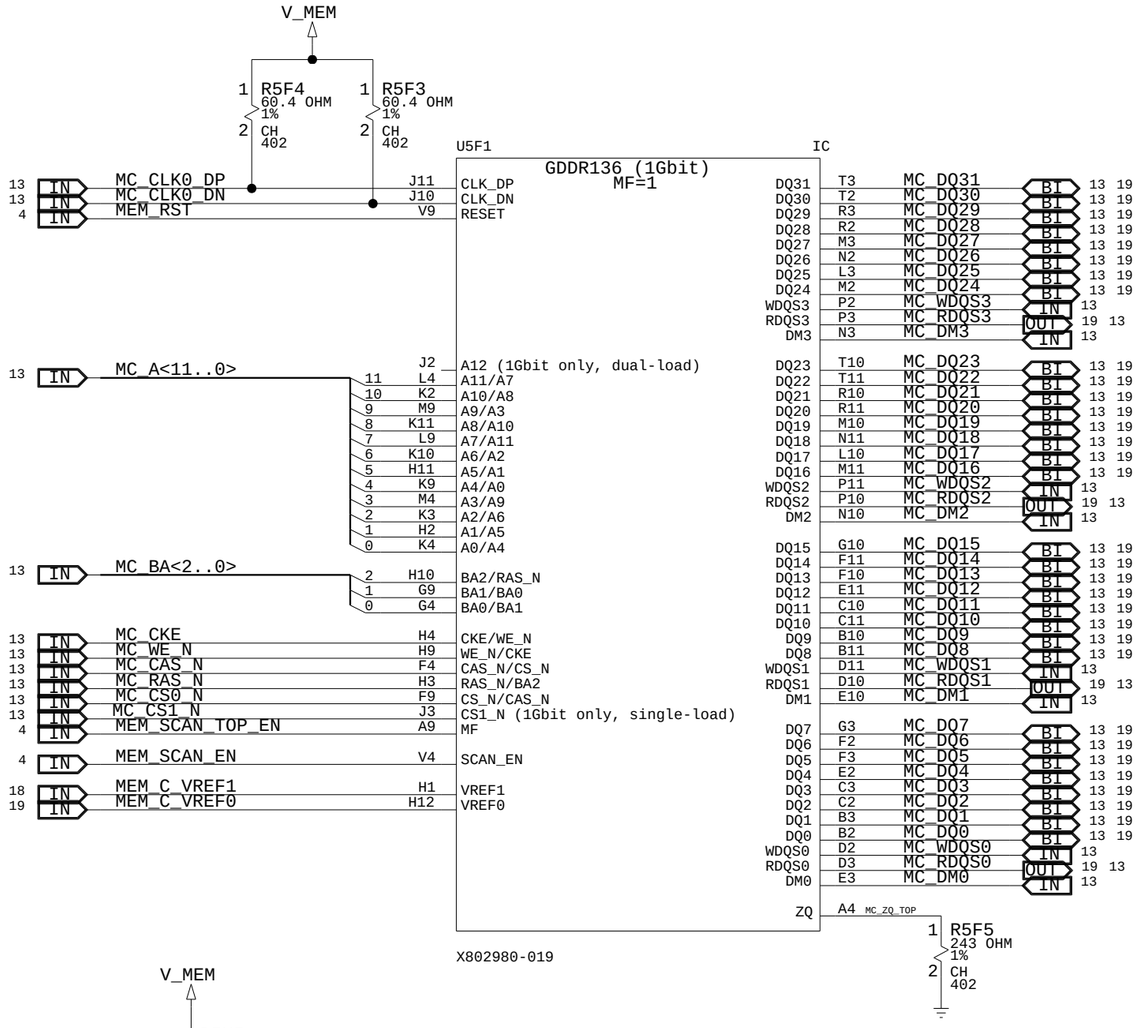
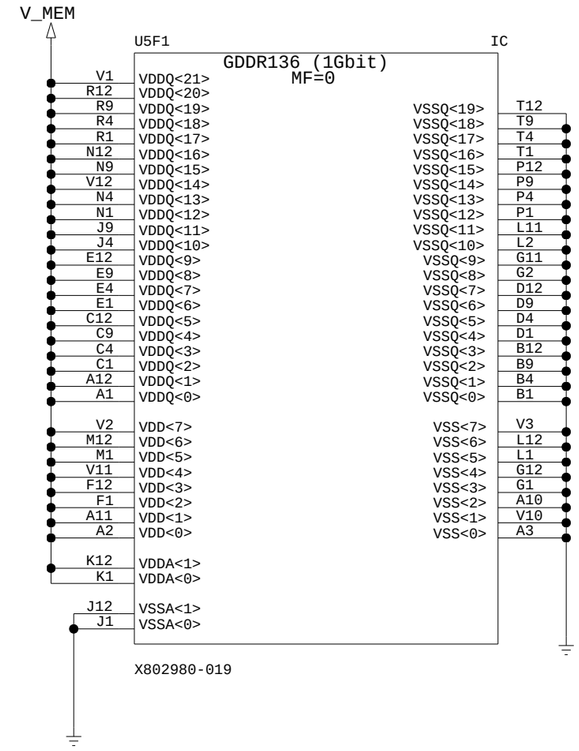
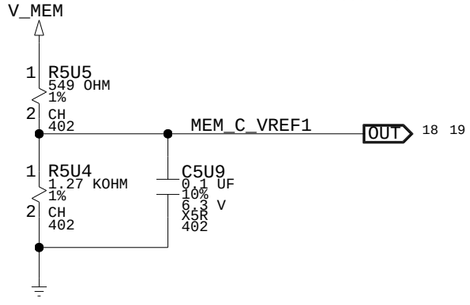
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	17/87	E	1.01

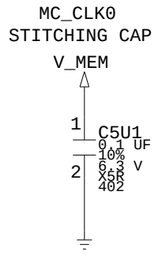
MEMORY PARTITION C, TOP

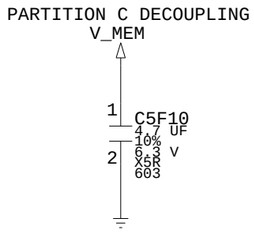
CHIP SELECT = 0, MIRROR FUNCTION = 0

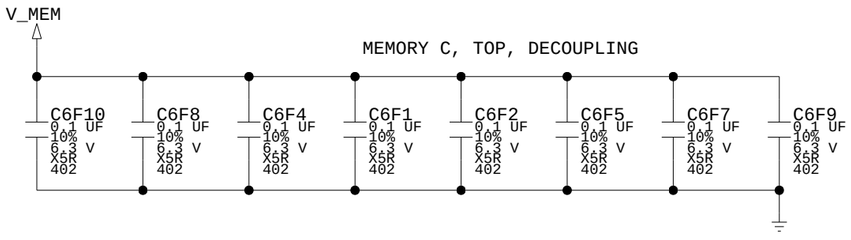












[PAGE_TITLE=MEMORY PARTITION C, TOP]

DRAWING
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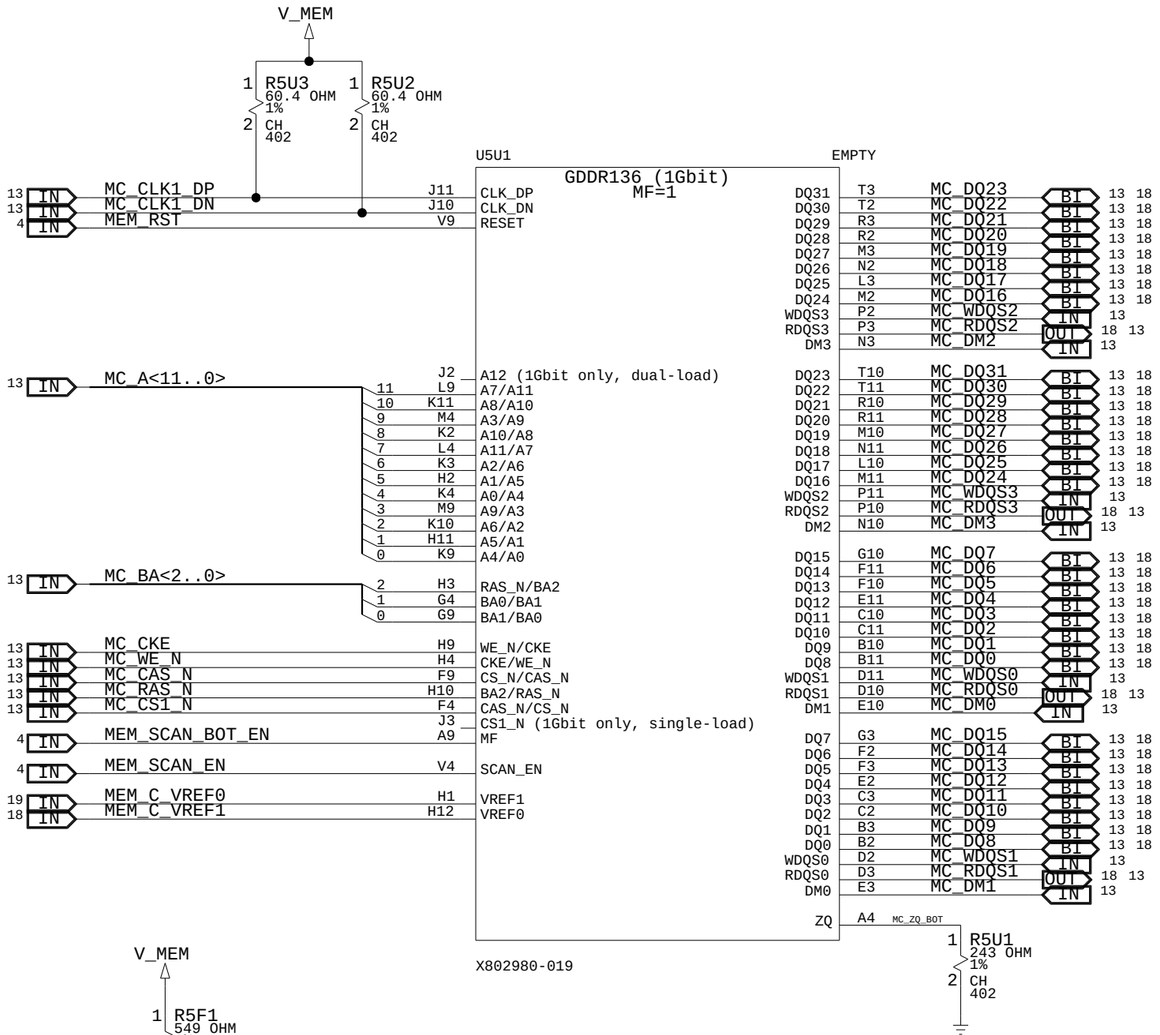
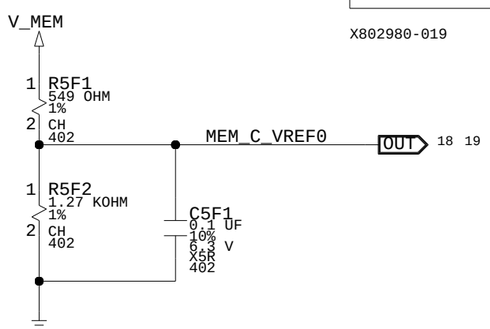
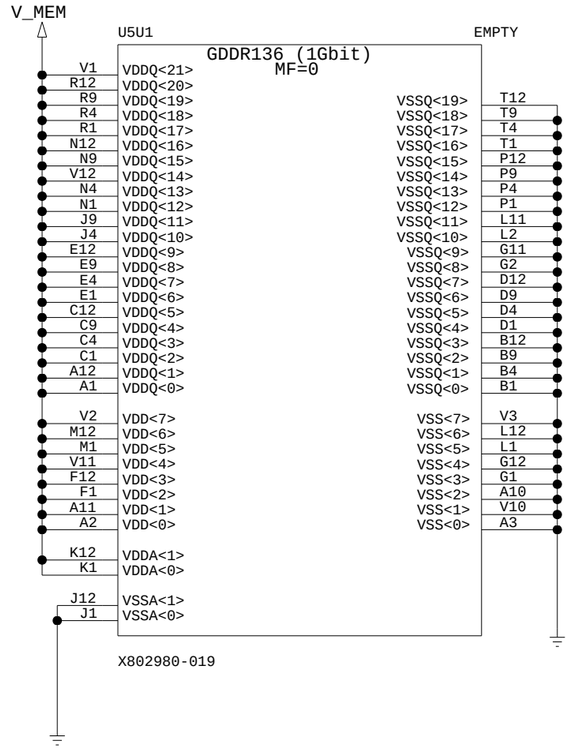
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	18/87	E	1.01

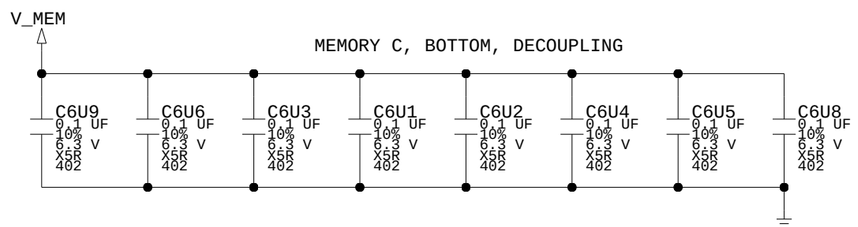
MEMORY PARTITION C, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1









[PAGE_TITLE=MEMORY PARITION C, BOTTOM]

DRAWING
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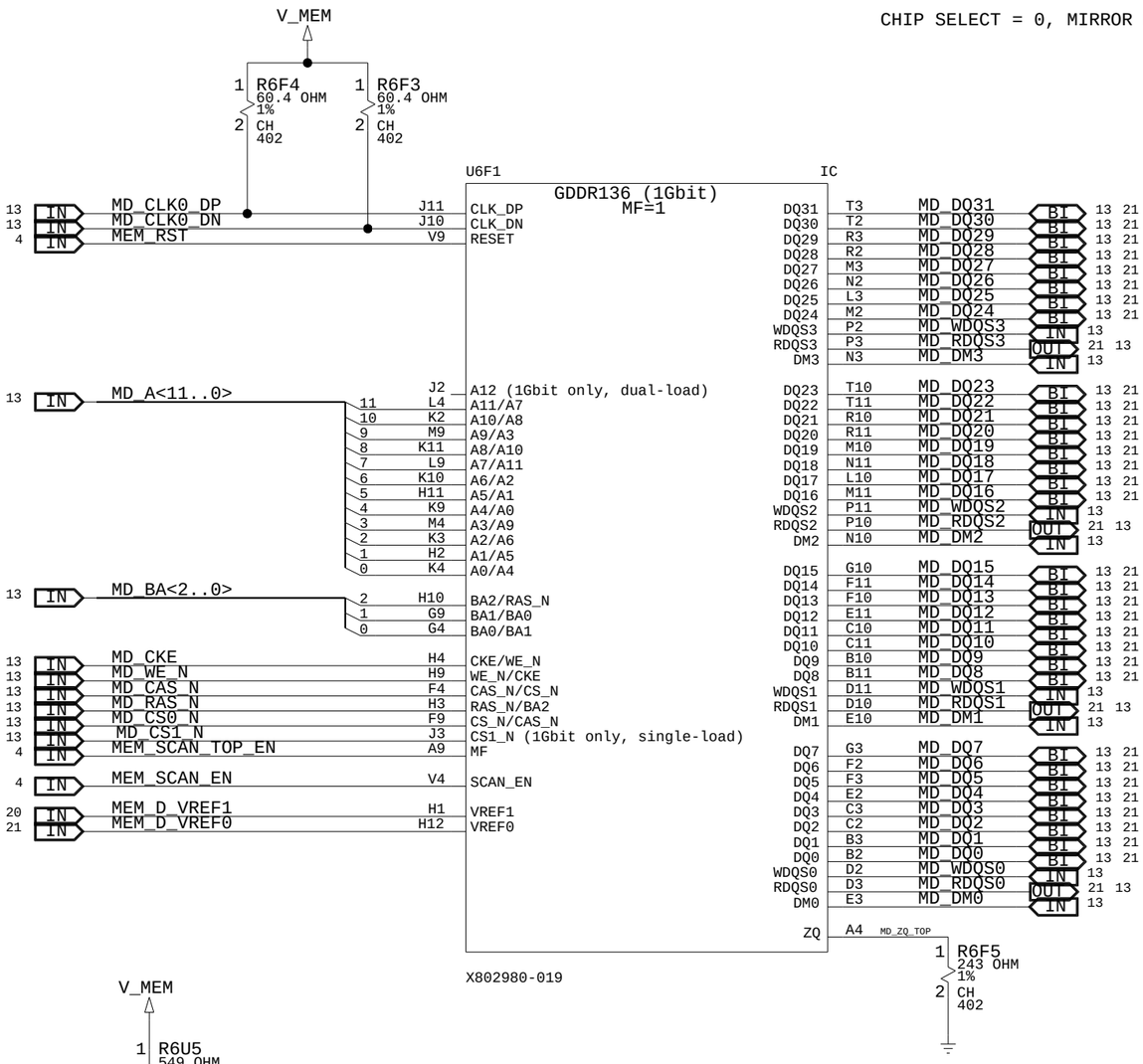
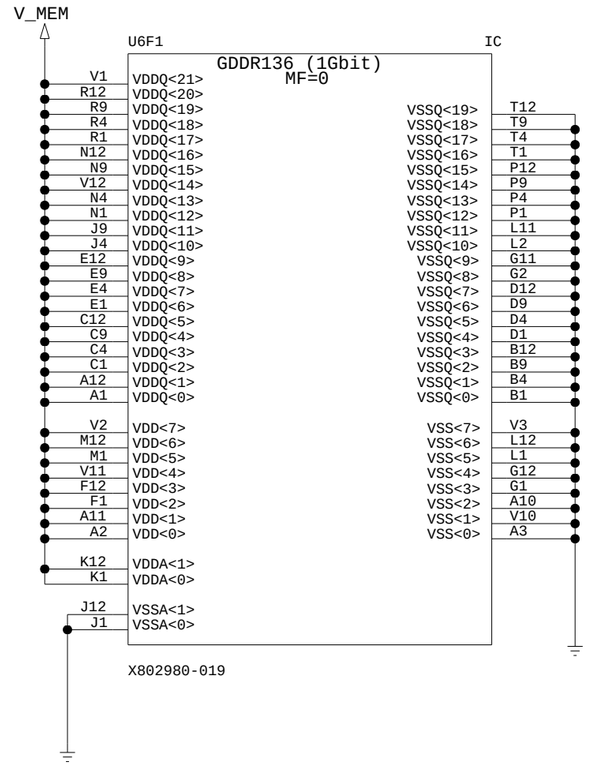
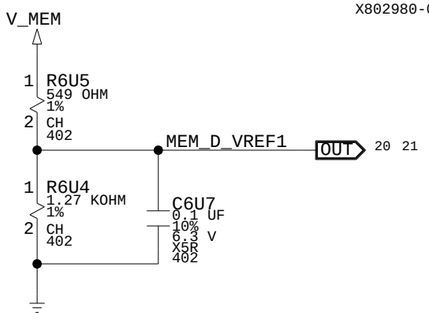
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	19/87	E	1.01

MEMORY PARTITION D, TOP

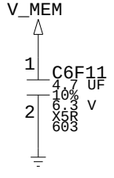
CHIP SELECT = 0, MIRROR FUNCTION = 0

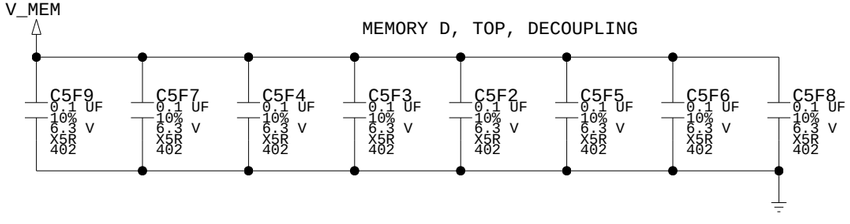






PARTITION D DECOUPLING





[PAGE_TITLE=MEMORY PARTITION D, TOP]

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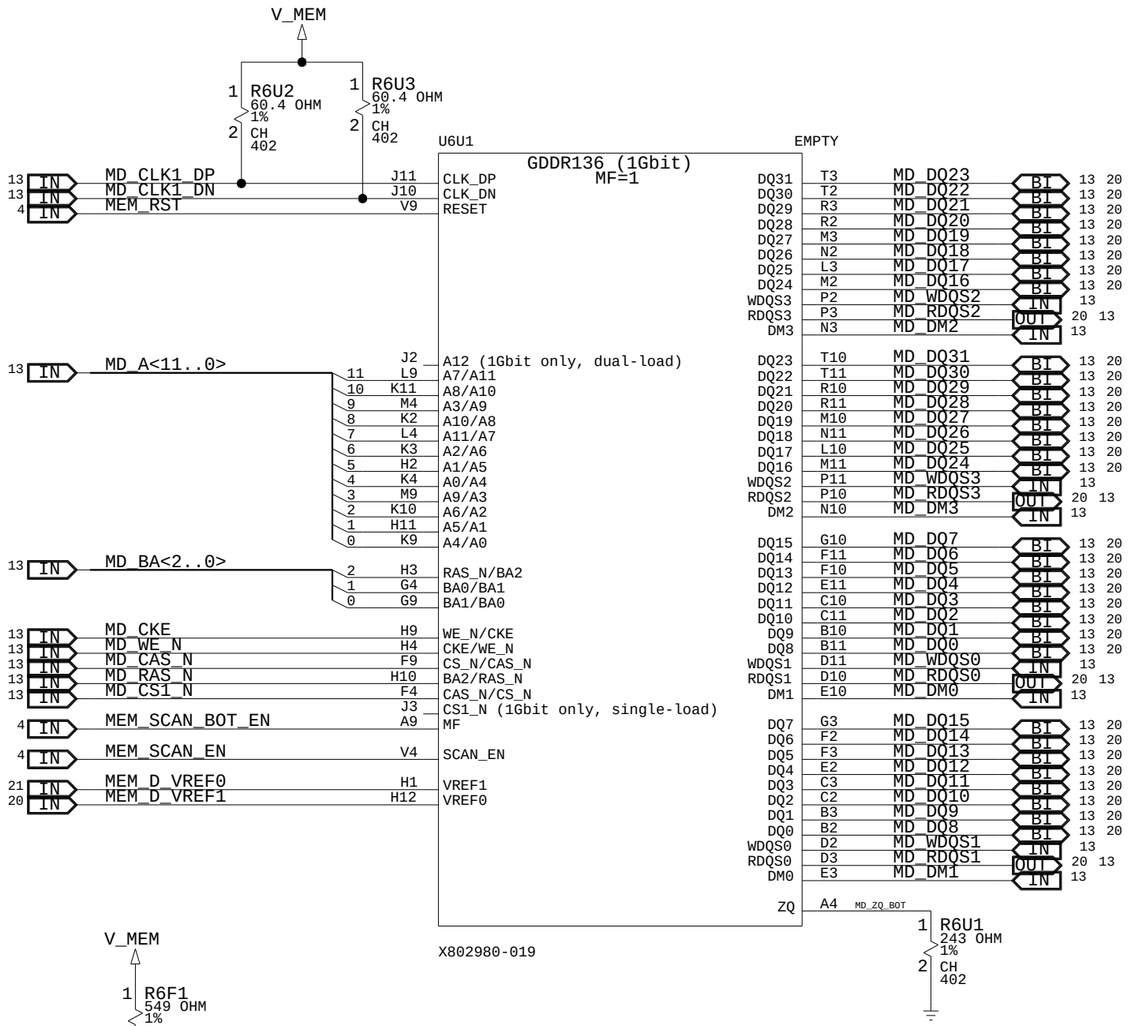
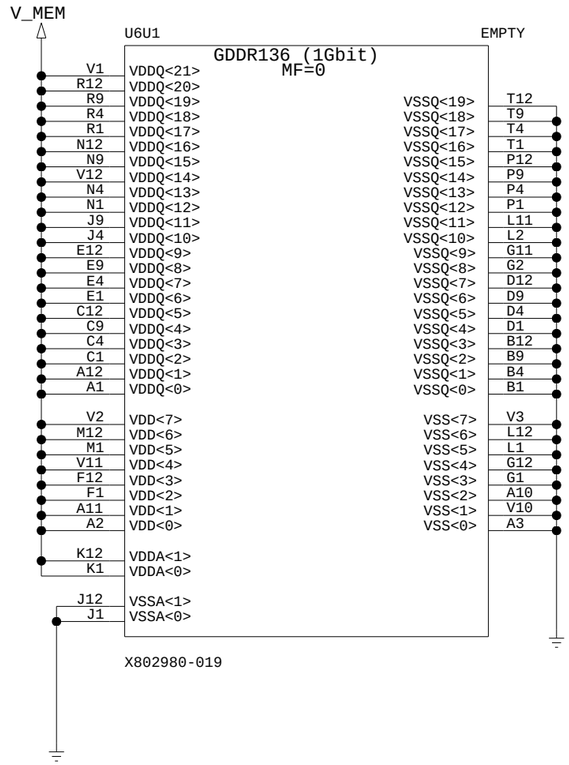
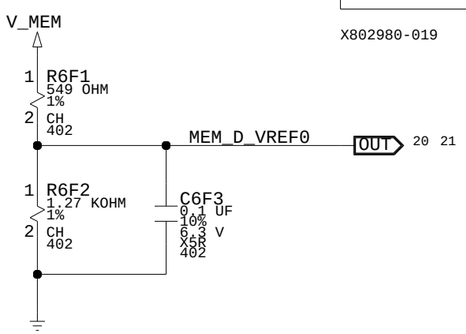
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	20/87	E	1.01

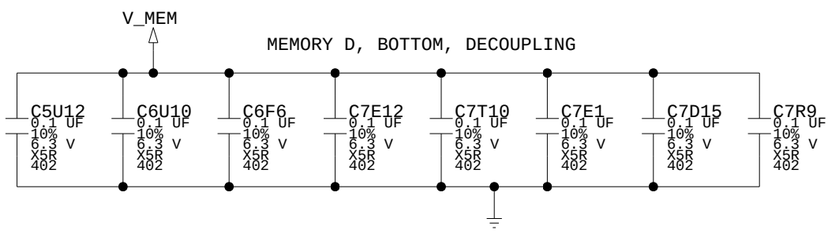
MEMORY PARTITION D, BOTTOM

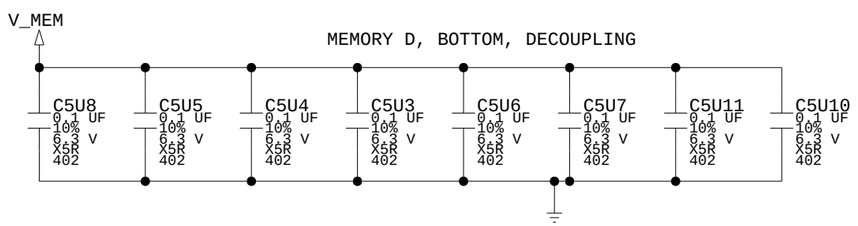
CHIP SELECT = 1, MIRROR FUNCTION = 1











[PAGE_TITLE=MEMORY PARTITION D, BOTTOM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	21/87	E	1.01

KSB, CLOCKS + STRAPPING + POR

XTAL BYPASS: STUFF R3, R4, R5, AND C153 AND
APPLY SQUARE WAVE TO XTAL_IN (VL=0V VH=1V)
KEEP R5 CLOSE TO KSB CHIP

RESISTOR VALUES CHOSEN TO GIVE V_12P0_DET 1P8V NOMINAL

V_12P0
R3R5 1% 84.52 KOHM CH 402
R3R17 1% 15 KOHM CH 402
C3R55 470 PF 5% 50 V EMPTY 402
R3D26 49.9 OHM 1% EMPTY 402
DB3D2
Y3D1 25 MHZ SM XTAL
C3D7 27 PF 5% 50 V COG 402
C3D8 27 PF 5% 50 V NPO 402
V_3P3STBY
R3D17 8.25 KOHM 1% EMPTY 402
R3D19 1.5 KOHM 1% EMPTY 402
C3D1 0.01 UF 10% 16 V EMPTY 402
DB2C2

U3D1 KSB IC
1 OF 9

V_12P0_DET	W20	V_12P0_DET	V_12P0_OK
POR_BYPASS	B4	POR_BYPASS<DN>	V_RST_OK<DN>
			MAIN_PWR_OK
			SB_RST_N*
XTAL_IN	AB21	XTAL_IN	SMC_RST_N_OUT
XTAL_OUT	AA21	XTAL_OUT	
	AA22	XTAL_VSS	
EXT_CLK48_IN	Y20	CLK48<DN>	
EXT_CLK48_SEL	W19	CLK48_BYPASS<DN>	
SMB_DATA	A4	SMB_DATA	
SMB_CLK	A5	SMB_CLK	

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	C5	V19	V12P0_PWRGD
	C4		V_RST_OK
	C9	SB_RST_N_R	SB_MAIN_PWRGD
	D7	SMC_RST_N_R	
CPU_CLK_DP	U21	CPU_CLK_DP_R	
CPU_CLK_DN	V21	CPU_CLK_DN_R	
NB_CLK_DP	V22	GPU_CLK_DP_R	
NB_CLK_DN	W22	GPU_CLK_DN_R	
PCIEX_CLK_IN_DP	Y15	EXT_PCIEX_CLK_DP	
PCIEX_CLK_IN_DN	AA15	EXT_PCIEX_CLK_DN	
PIX_CLK_OUT_DP	U22	PIX_CLK_2X_DP_R	
PIX_CLK_OUT_DN	T22	PIX_CLK_2X_DN_R	

V12P0_PWRGD OUT 25 42
FTP FT2P6
V_RST_OK OUT
FTP FT3R3
SB_MAIN_PWRGD IN 25
FTP FT3P5
R3P2 1 KOHM 5% CH 402
SB_RST_N IN 25
R2P3 10 KOHM 5% CH 402
R3P15 10 KOHM 5% CH 402
R3P16 1 KOHM 5% CH 402
SMC_RST_N OUT 25 42 62
R3D6 33 OHM 5% CH 402
R3D7 49.9 OHM 1% CH 402
CPU_CLK_DP OUT 2
CPU_CLK_DN OUT 2
R3D8 33 OHM 5% CH 402
R3D9 49.9 OHM 1% CH 402
R3D10 33 OHM 5% CH 402
R3D11 49.9 OHM 1% CH 402
GPU_CLK_DP OUT 4 62
R3D12 33 OHM 5% CH 402
R3D13 49.9 OHM 1% CH 402
GPU_CLK_DN OUT 4 62
V_3P3
R3D28 10 KOHM 1% CH 402
R3D29 10 KOHM 1% CH 402
DB3R6
DB3R7
R3D5 33 OHM 5% CH 402
R3D14 60.4 OHM 1% CH 402
PIX_CLK_2X_DP OUT 4
PIX_CLK_2X_DN OUT 4
R3D3 33 OHM 5% CH 402
R3D4 60.4 OHM 1% CH 402
FTP FT3R7
FTP FT3R2

SMB_DATA BI 62 61 55 25
SMB_CLK BI 62 61 55 25

I2C ADDRESS

	0011 100 R/W HEX	0111 000 R/W HEX
WRITE	0011 100 0 0X38	0111 000 0 0X70
READ	0011 100 1 0X39	0111 000 1 0X71

	0011 110 R/W HEX
WRITE	0011 110 0 0X3C
READ	0011 110 1 0X3D

[PAGE_TITLE=KSB, CLOCKS + STRAPING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	22/87	E	1.01

KSB, VIDEO + FAN

U3D1 KSB IC

2 OF 9

4 IN GPU_PIX_CLK_1X → J20 PIX_CLK_IN

4 IN PIX_DATA<14..0>

14	G20	PIX_DATA14
13	G21	PIX_DATA13
12	G22	PIX_DATA12
11	H20	PIX_DATA11
10	H21	PIX_DATA10
9	H22	PIX_DATA9
8	J21	PIX_DATA8
7	J22	PIX_DATA7
6	K21	PIX_DATA6
5	K22	PIX_DATA5
4	K20	PIX_DATA4
3	L21	PIX_DATA3
2	L22	PIX_DATA2
1	L20	PIX_DATA1
0	M20	PIX_DATA0

4 IN GPU_HSYNC_OUT → M22 HSYNC_IN

4 IN GPU_VSYNC_OUT → M21 VSYNC_IN

DAC_RSET → D20 DAC_RSET

1 R3P11 5.11 KOHM 0.1% 2 CH 402

DAC_D_OUT_DP A20 VID_DACD_DP → OUT 37

DAC_D_OUT_DN F18

DAC_B_OUT_DP A21 VID_DACB_DP → OUT 37

DAC_B_OUT_DN G18

DAC_A_OUT_DP C22 VID_DACA_DP → OUT 37

DAC_A_OUT_DN G19

DAC_C_OUT_DP D22 VID_DACC_DP → OUT 37

DAC_C_OUT_DN H18

HSYNC_OUT B19 VID_HSYNC_OUT_R → OUT 37

VSYNC_OUT C19 VID_VSYNC_OUT_R → OUT 37

61 IN BRD_TEMP_P — R4G2 1 2 — BRD_TEMP_P_DIODE — Q4G1 EMPTY

0 OHM 5% 402 EMPTY

61 38 OUT BRD_TEMP_N — R4G1 1 2 — BRD_TEMP_N_DIODE

0 OHM 5% 402 EMPTY

40 IN HDMI_HPD → D18 HDMI_HPD

KSB_RSET → H4 RSET

1 R2P4 2 KOHM 1% 2 CH 402

FT3P1 FTP 1

25 IN SMC_PWM0 — 2 R3P3 1 — 205 KOHM 1% 402 EMPTY — FAN_OP1_DP → F22 FAN_OP1_DP

1 C3P2 0.22 UF 10% 6.3 V EMPTY 402 2

36 IN FAN1_FDBK → F21 FAN_OP1_DN

64 61 IN CPU_TEMP_N_KSB — ST3C5 2 1 SHORT

64 61 IN GPU_TEMP_N_KSB — ST3C2 2 1 SHORT → P22 TEMP_N

64 61 IN EDRAM_TEMP_N_KSB — ST3C4 2 1 SHORT

61 IN BRD_TEMP_N_KSB — ST3C3 2 1 SHORT

23 IN CAL_TEMP_N — ST3C1 2 1 SHORT

TMDS_TXC_DP A16 HDMI_TXC_DP — C3C4 2 1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TXC_DP_R — R3C23 2 1 301 OHM 1% 603 EMPTY → OUT 40

TMDS_TXC_DN B16 HDMI_TXC_DN → OUT 40

TMDS_TX2_DP B13 HDMI_TX2_DP — C3C1 2 1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX2_DP_R — R3C20 2 1 301 OHM 1% 603 EMPTY → OUT 40

TMDS_TX2_DN C13 HDMI_TX2_DN → OUT 40

TMDS_TX1_DP A14 HDMI_TX1_DP — C3C2 2 1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX1_DP_R — R3C21 2 1 301 OHM 1% 603 EMPTY → OUT 40

TMDS_TX1_DN B14 HDMI_TX1_DN → OUT

TMDS_TX0_DP B15 HDMI_TX0_DP — C3C3 2 1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX0_DP_R — R3C22 2 1 301 OHM 1% 603 EMPTY → OUT 40

TMDS_TX0_DN C15 HDMI_TX0_DN → OUT 40

DDC_SCK A12 HDMI_DDC_CLK ↔ BI 37 40 55

DDC_SDA B12 HDMI_DDC_DATA ↔ BI 37 40 55

1 DB3P1 1 DB3R1 1 DB3P2 1 DB3R2 — CUSTOM THERMAL CALIBRATION PADS LOCATION MUST REMAIN LOCKED

FAN_OUT1 E21 FAN1_OUT → OUT 36

1 C3R1 100 PF 5% 50 V EMPTY 402 2

TEMP3_P N22 CAL_TEMP_P — CAL_TEMP_N → OUT 23

TEMP2_P P20 GPU_TEMP_P_KSB → OUT 61 64

TEMP1_P P21 CPU_TEMP_P_KSB → OUT 61 64

TEMP0_P R21 EDRAM_TEMP_P_KSB → OUT 61 64

TEMP4_P N21 BRD_TEMP_P_KSB → OUT 61

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[PAGE_TITLE=KSB, VIDEO + FAN]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	23/87	E	1.01

KSB, PCIEX + SMM GPIO + JTAG

V_3P3

R2C14 10 KOHM 5% EMPTY 402
R2C12 10 KOHM 5% EMPTY 402
R2C18 10 KOHM 5% EMPTY 402
R2C16 10 KOHM 5% EMPTY 402
R2C20 10 KOHM 5% EMPTY 402
R2C13 1 KOHM 5% CH 402
R2C11 1 KOHM 5% CH 402
R2C17 1 KOHM 5% CH 402
R2C15 1 KOHM 5% CH 402
R2C19 1 KOHM 5% CH 402

SB_GPIO<0..15> BI 24 62

U3D1 KSB IC
4 OF 9

PEX_GPU_SB_L1_DP IN 4
PEX_GPU_SB_L1_DN IN 4
PEX_GPU_SB_L0_DP IN 4
PEX_GPU_SB_L0_DN IN 4

PEX_TX1_DP AA19 PEX_SB_GPU_L1_DP_C C3D5 0.1 UF 10% 6.3 V X5R 402 PEX_SB_GPU_L1_DP OUT 4 62
PEX_TX1_DN AB19 PEX_SB_GPU_L1_DN_C C3D6 0.1 UF 10% 6.3 V X5R 402 PEX_SB_GPU_L1_DN OUT 4 62
PEX_TX0_DP AA17 PEX_SB_GPU_L0_DP_C C3D3 0.1 UF 10% 6.3 V X5R 402 PEX_SB_GPU_L0_DP OUT 4 62
PEX_TX0_DN AB17 PEX_SB_GPU_L0_DN_C C3D4 0.1 UF 10% 6.3 V X5R 402 PEX_SB_GPU_L0_DN OUT 4 62

Y18 PEX_RX1_DP
AA18 PEX_RX1_DN
Y16 PEX_RX0_DP
AA16 PEX_RX0_DN

V_3P3STBY

R3G19 10 KOHM 5% CH 402
R2C21 0 OHM 5% 402 CH
R2C1 10 KOHM 5% EMPTY 402

24 IN AUD_SPI_MOSI_R
AUD_SPI_MOSI OUT 35

62 IN KER_DBG_RXD A3 UART0_RXD<UP>

UART0_TXD A2 KER_DBG_TXD_R R2C9 47 OHM 5% 402 CH KER_DBG_TXD OUT 62

TST_PT E18 KSB_DEBUG 1 DB3P3

V_3P3STBY

R3G18 10 KOHM 5% CH 402
R2C25 0 OHM 5% 402 CH
R2C24 10 KOHM 5% EMPTY 402

62 24 OUT AUD_SPI_MISO_R
AUD_SPI_MISO IN 35

GPIO<1> = 0 ENABLE DEBUG OUTPUT
1 DISABLE DEBUG OUTPUT

GPIO<0,2,3> = 111 XENON
110 ZEPHYR A
101 ZEPHYR B
100 ZEPHYR C
011 FALCON
010 JASPER
001 TRINITY
000 CORONA

GPIO15 F2 AUD_SPI_MISO_R IN 24
GPIO14 F3 AUD_SSB_R OUT 24 62
GPIO13 E1 SCART_RGB OUT 37 62
GPIO12 E4 AUD_RST_N OUT 33
GPIO11 E3 AUD_RDY_BSBY_R OUT 24 62
GPIO10 F4 62 FAN_TACH_SMM_R
GPIO9 G4 WSS_CNTL0 OUT 37 62
GPIO8 G3 WSS_CNTL1 OUT 37 62
GPIO7 D3 AUD_SPI_MOSI_R OUT 24 62
GPIO6 D4 AUD_SPI_CLK_R OUT 24 62
GPIO5 E2 SB_GPIO<5> BI 24 62
GPIO4 C1 SB_GPIO<4> OUT 24 62
GPIO3 C2 SB_GPIO<3> OUT 24 62
GPIO2 D1 SB_GPIO<2> OUT 24 62
GPIO1 B1 SB_GPIO<1> BI 24 62
GPIO0 B2 SB_GPIO<0> OUT 24 62

R2P9 5% 0 OHM CH 402 FAN_TACH IN 36

V_3P3STBY

R3G3 10 KOHM 5% CH 402
R2C23 0 OHM 5% 402 CH
R2C22 10 KOHM 5% EMPTY 402

24 IN AUD_SPI_CLK_R
AUD_SPI_CLK OUT 35

63 IN SB_TCLK T19 TCK<DN>
63 OUT SB_TDO R19 TDO
63 IN SB_TDI R20 TDI<UP>
63 IN SB_TMS U19 TMS<UP>
63 IN SB_TRST N19 TRST<DN>

FT3T8 FTP
FT3T7 FTP
FT3T6 FTP
FT3T5 FTP
FT3T4 FTP

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V_3P3STBY

R2G6 10 KOHM 5% CH 402
R2G5 0 OHM 5% 402 CH
R2G7 10 KOHM 5% EMPTY 402

24 IN AUD_RDY_BSBY_R
AUD_RDY_BSBY OUT 35

V_3P3STBY

R3G20 10 KOHM 5% CH 402
R2P5 0 OHM 5% 402 CH
R2C26 10 KOHM 5% EMPTY 402

24 IN AUD_SSB_R
AUD_SSB OUT 35

DEBUG BUS

NET NAME	DEBUG BUS BIT
SB_GPIO<0>	0
SB_GPIO<2>	1
SB_GPIO<3>	2
SB_GPIO<4>	3
AUD_SPI_CLK_R	4
SB_GPIO<5>	5
WSS_CNTL1	6
WSS_CNTL0	7
FAN_TACH	8
AUD_RDY_BSBY_R	9
SCART_RGB	10
AUD_SSB_R	11
AUD_SPI_MISO_R	12

[PAGE_TITLE=KSB, PCIEX + SMM GPIO + JTAG]

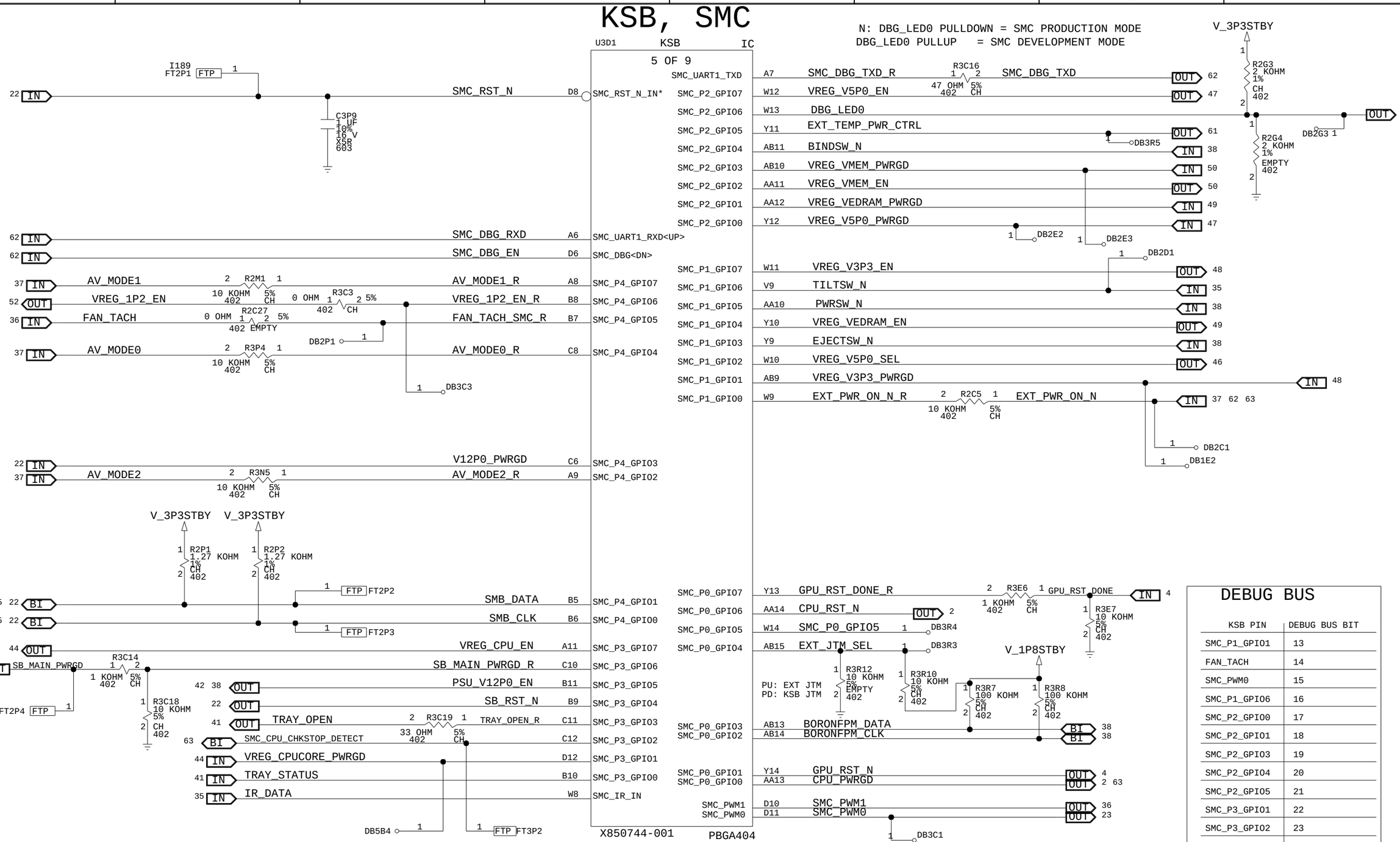
DRAWING
Thu Feb 17 10:12:24 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	24/87	E	1.01

KSB, SMC

N: DBG_LED0 PULLDOWN = SMC PRODUCTION MODE
DBG_LED0 PULLUP = SMC DEVELOPMENT MODE

U3D1 KSB IC
5 OF 9



DEBUG BUS

KSB PIN	DEBUG BUS BIT
SMC_P1_GPIO1	13
FAN_TACH	14
SMC_PWM0	15
SMC_P1_GPIO6	16
SMC_P2_GPIO0	17
SMC_P2_GPIO1	18
SMC_P2_GPIO3	19
SMC_P2_GPIO4	20
SMC_P2_GPIO5	21
SMC_P3_GPIO1	22
SMC_P3_GPIO2	23

SMC_P1,2,3,4 GPIOS ARE ON V3P3STBY. SMC_P0 GPIOS ARE ON 1P8VSTBY

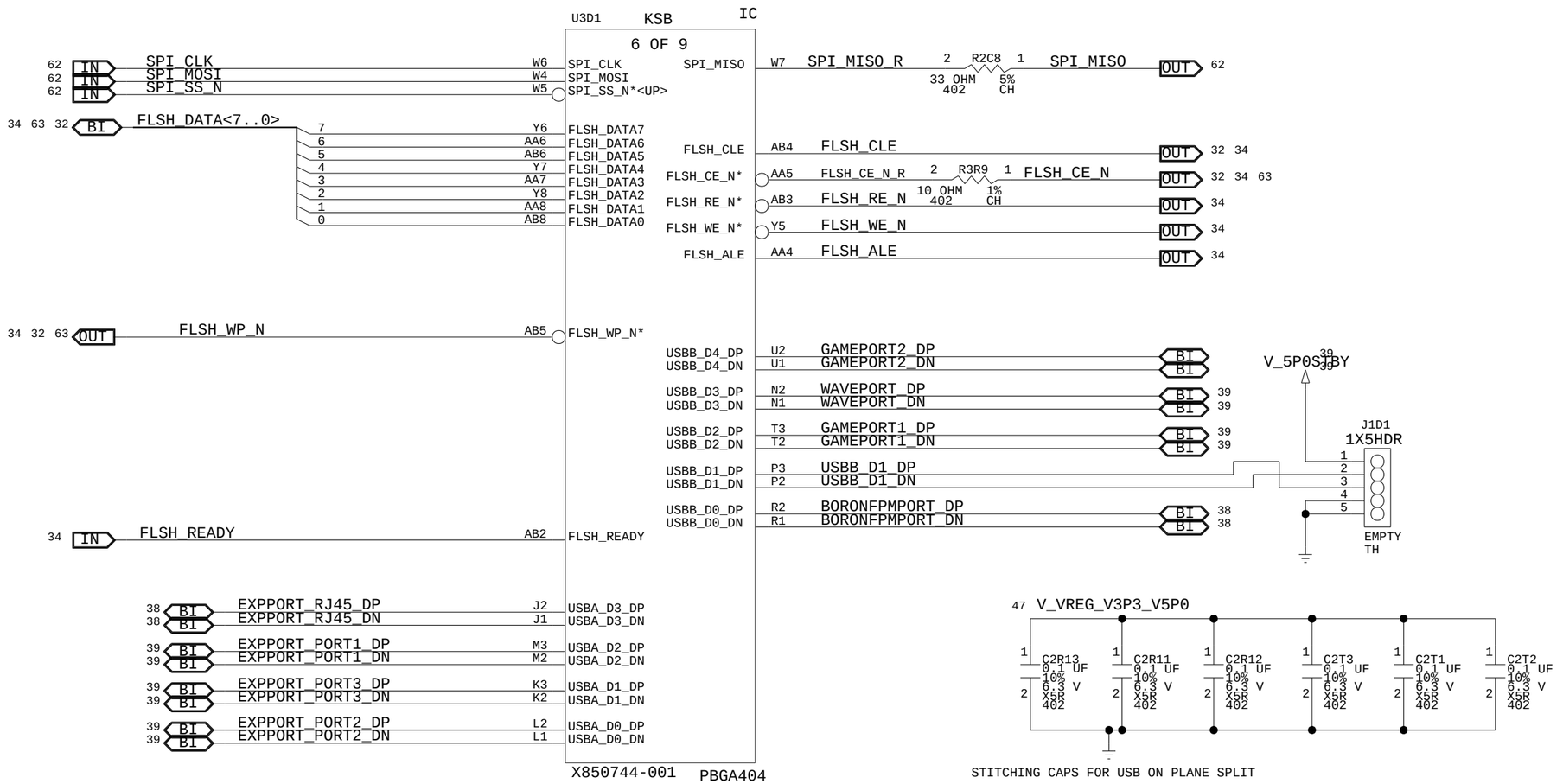
[PAGE_TITLE=KSB, SMC]

DRAWING
Thu Feb 17 10:12:24 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	25/87	E	1.01

KSB, FLASH + USB + SPI

N: ALL PORTS ARE DIFFERENTIAL USB PAIRS ON THIS PAGE



[PAGE_TITLE=KSB, FLASH + USB + SPI]

DRAWING
Thu Feb 17 10:12:24 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	26/87	E	1.01

KSB, ETHERNET + AUDIO + SATA

V_3P3STBY

C3P32 0.1 UF 10% 6.3 V X5R 402
C3P35 0.1 UF 10% 6.3 V X5R 402
C3P33 0.1 UF 10% 6.3 V X5R 402
C3P34 0.1 UF 10% 6.3 V X5R 402

V_1P2STBY

STITCHING CAPS FOR I2S SIGNALS,PARTICULARLY MCLK.
PLACE AS CLOSE AS POSSIBLE TO I2S_MCLK, I2S_BCLK, I2S_SD, AND I2S_WS.

U3D1 KSB IC
7 OF 9

38 B1	ENET_RX_DN	H2	MDIN1	MDIN0	G1	ENET_TX_DN	B1 38
38 B1	ENET_RX_DP	H3	MDIP1	MDIP0	G2	ENET_TX_DP	B1 38
			I2S_MCLK_OUT		B18	I2S_MCLK_R	R3P14 47 OHM 402 5% CH I2S_MCLK OUT 33
			I2S_BCLK_OUT		B17	I2S_BCLK_R	R3P10 47 OHM 402 5% CH I2S_BCLK OUT 33
			I2S_SD		A17	I2S_SD_R	R3P9 47 OHM 402 5% CH I2S_SD OUT 33
			I2S_WS		C17	I2S_WS_R	R3P8 47 OHM 402 5% CH I2S_WS OUT 33
41 IN	HDD_RX_DP	Y2	SATA1_RX_DP	SPDIF_OUT	D16	SPDIF_OUT_R	R3P20 0 OHM 402 5% CH SPDIF_OUT OUT 37 39
41 IN	HDD_RX_DN	Y3	SATA1_RX_DN				
41 IN	ODD_RX_DP	V2	SATA0_RX_DP				
41 IN	ODD_RX_DN	V3	SATA0_RX_DN				

R3P12 10 KOHM 5% CH 402
R3P13 10 KOHM 5% CH 402
R3P19 10 KOHM 5% CH 402

SATA1_TX_DP	AA2	HDD_TX_DP	OUT 41
SATA1_TX_DN	AA1	HDD_TX_DN	OUT 41
SATA0_TX_DP	W2	ODD_TX_DP	OUT 41
SATA0_TX_DN	W1	ODD_TX_DN	OUT 41

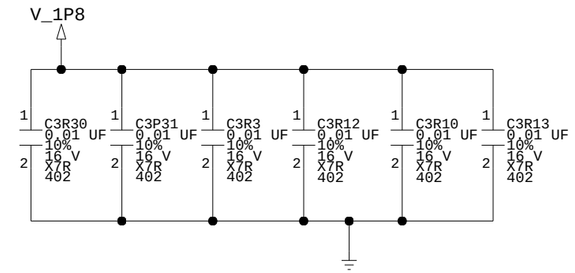
X850744-001 PBGA404

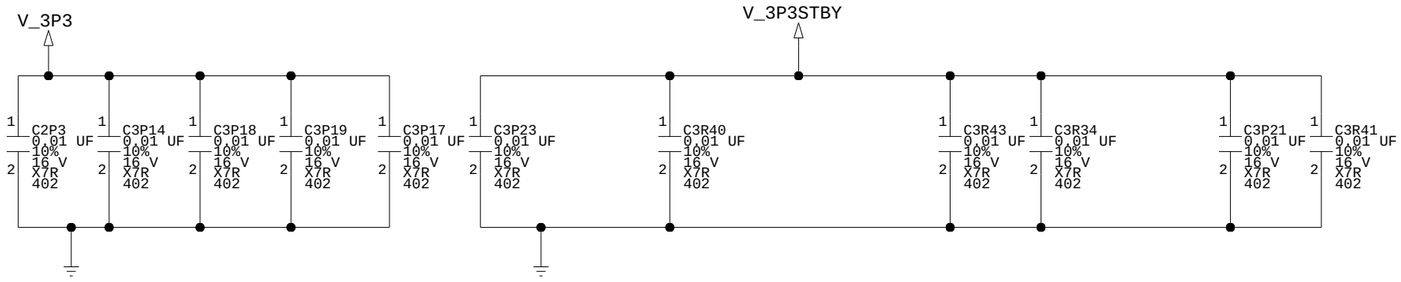
[PAGE_TITLE=KSB, ETHERNET + AUDIO + SATA]

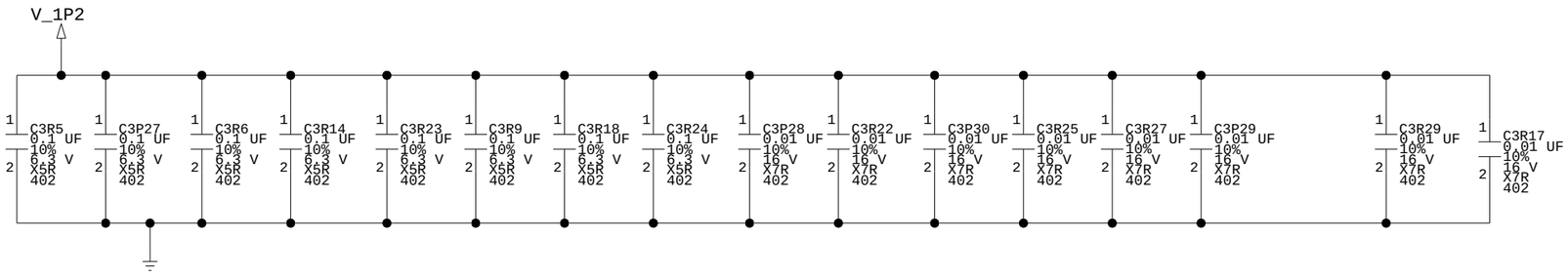
DRAWING
Thu Feb 17 10:12:25 2011

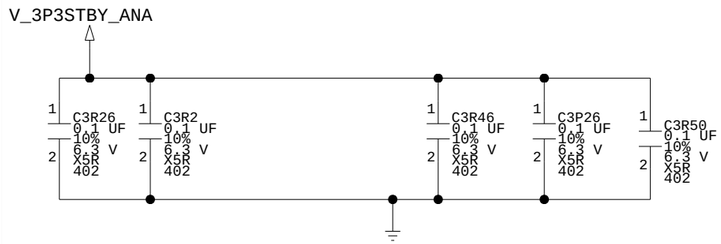
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	27/87	E	1.01

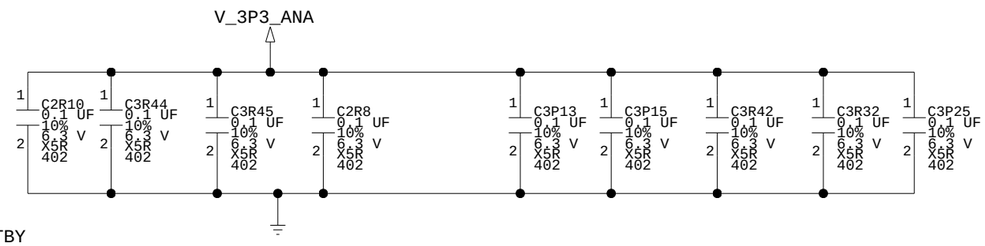
KSB,DECOUPLING

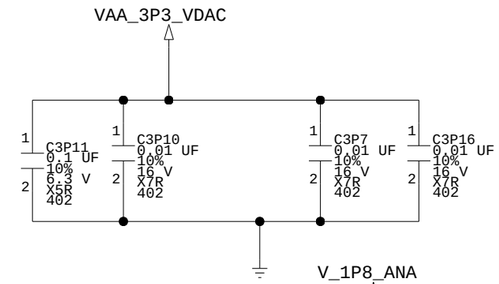


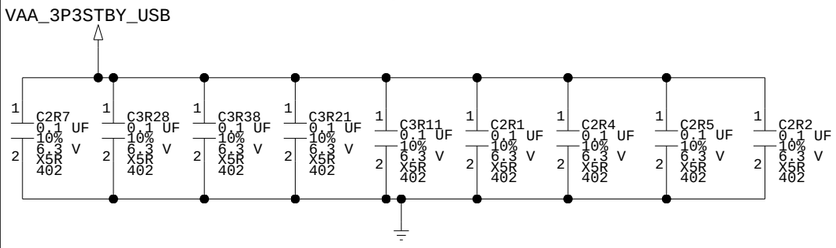


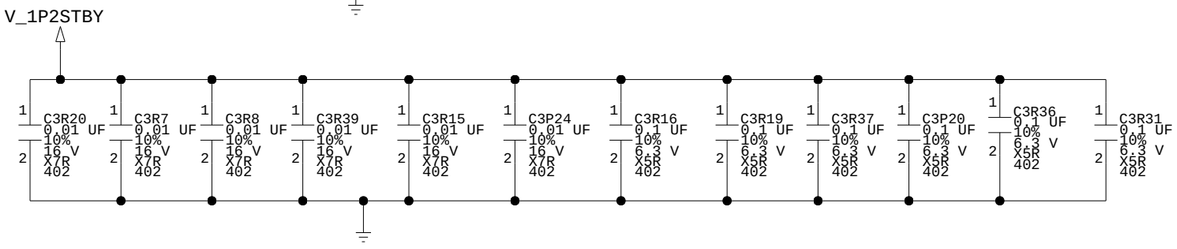


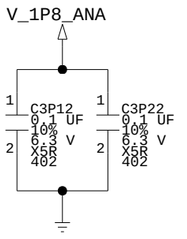










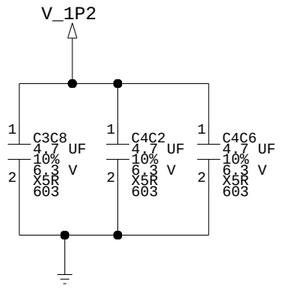


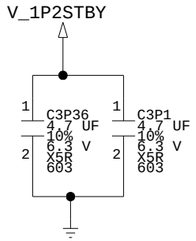
[PAGE_TITLE=KSB, DECOUPLING]

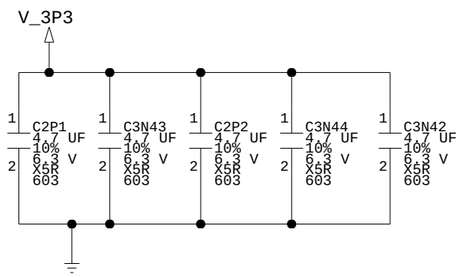
DRAWING
Thu Feb 17 10:12:24 2011

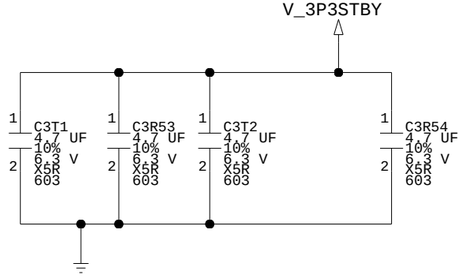
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	28/87	E	1.01

KSB, BULK DECOUPLING







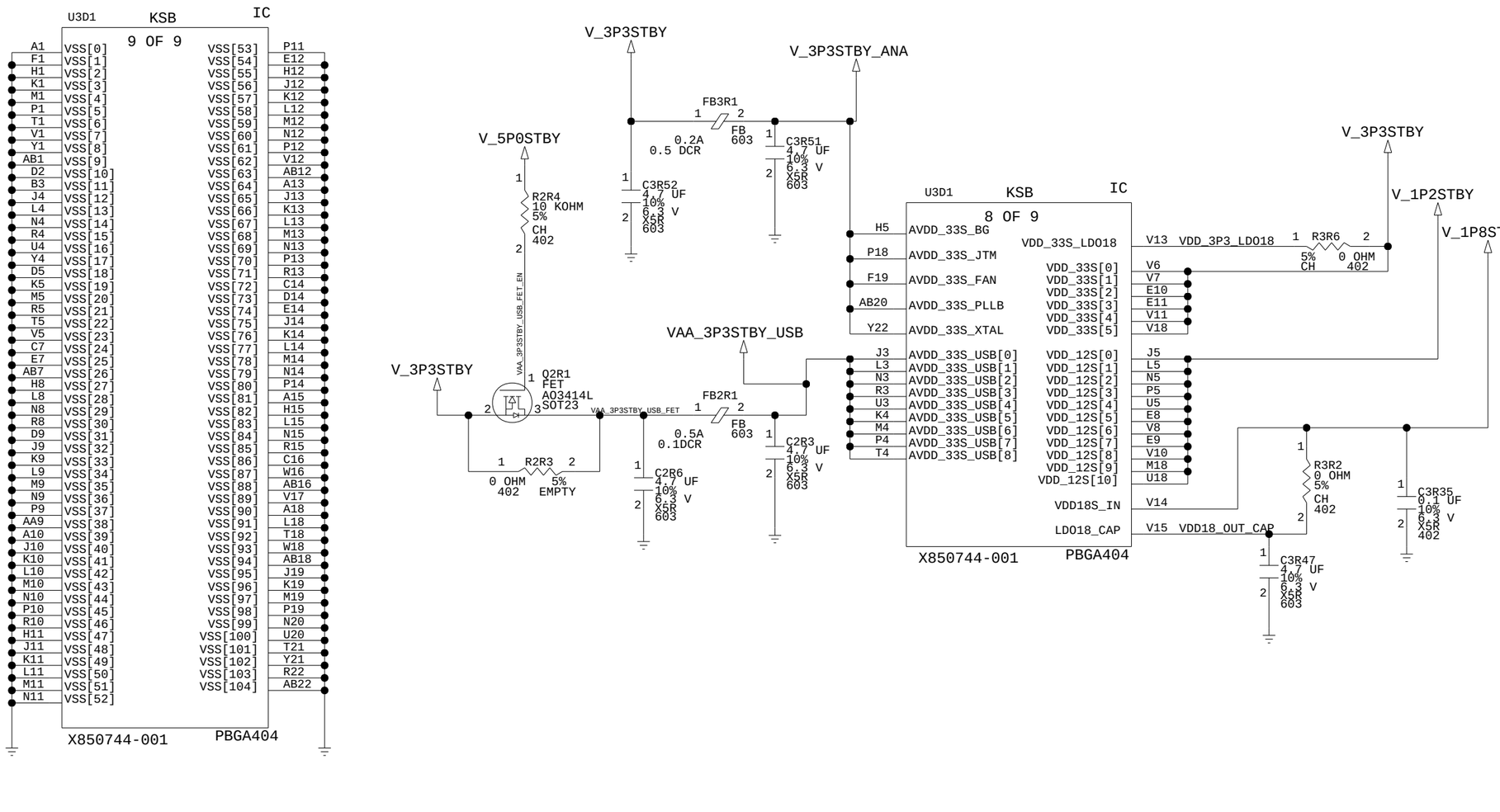


[PAGE_TITLE=KSB, BULK DECOUPLING]

DRAWING
Thu Feb 17 10:12:25 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	29/87	E	1.01

KSB, STANDBY POWER + GROUND

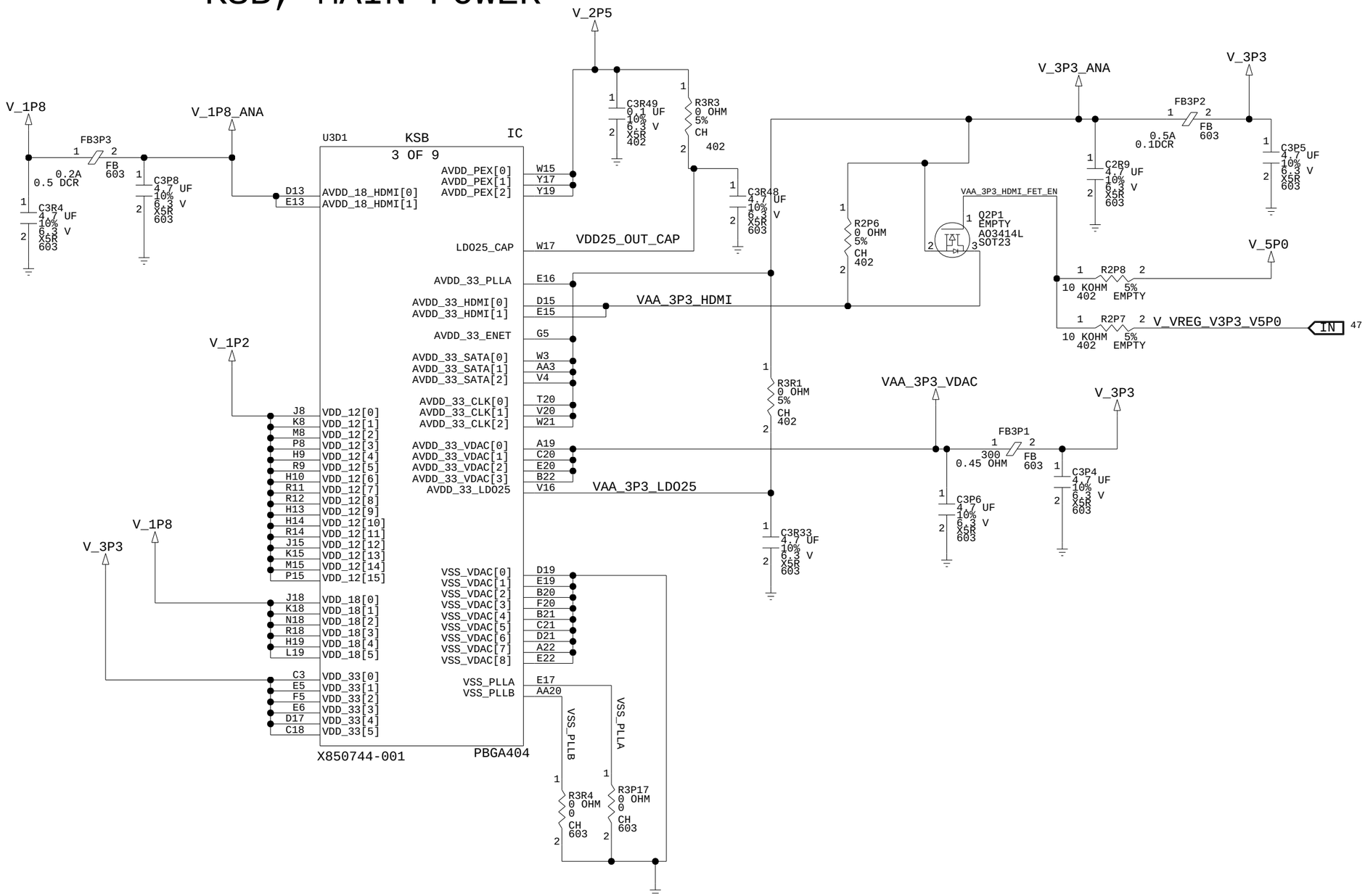


[PAGE_TITLE=KSB, STANDBY POWER]

DRAWING
Thu Feb 17 10:12:17 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	30/87	E	1.01

KSB, MAIN POWER



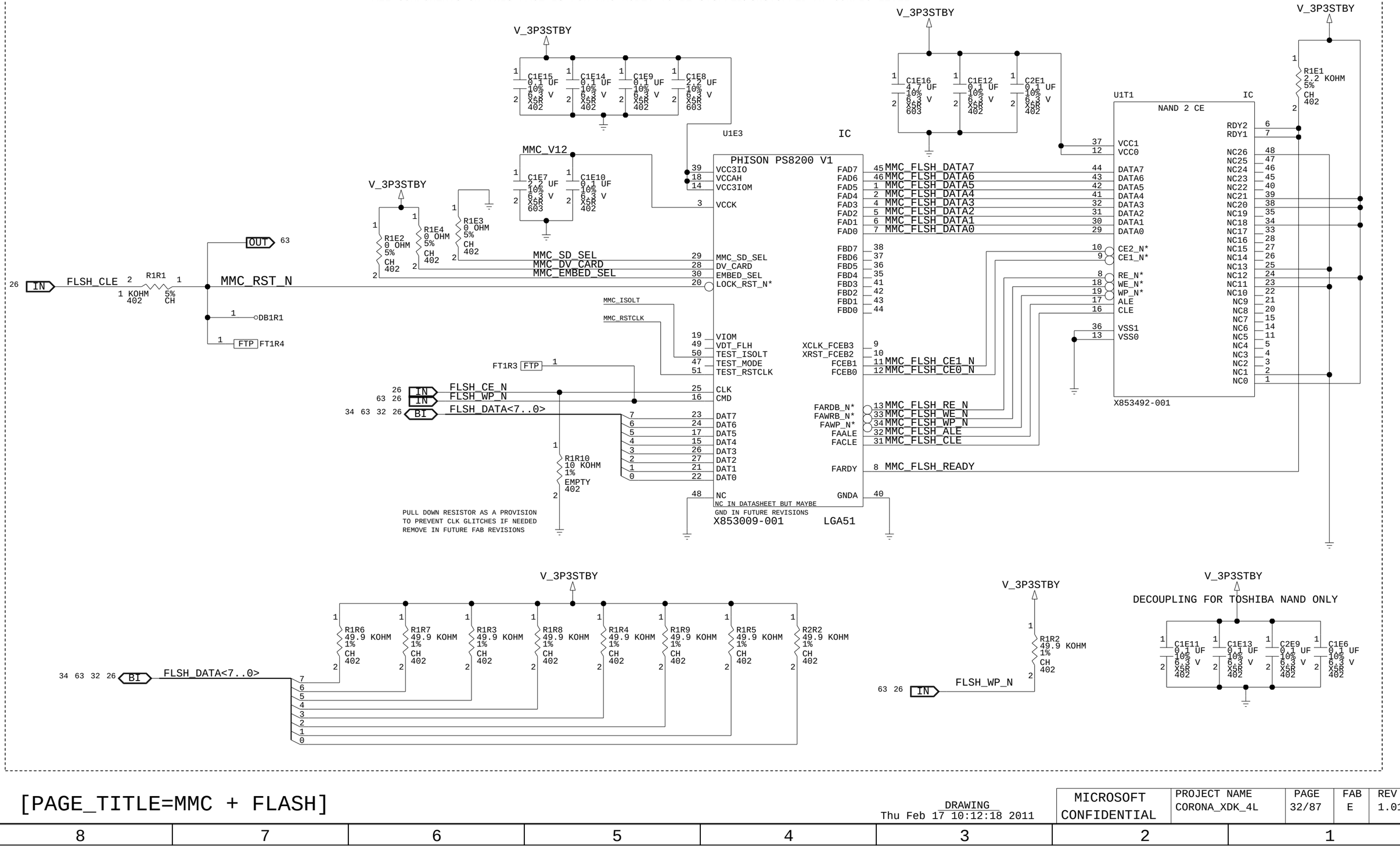
[PAGE_TITLE=KSB, MAIN POWER]

DRAWING
Thu Feb 17 10:12:18 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	31/87	E	1.01

MMC + FLASH

ALL COMPONENTS ON THIS PAGE IS FOR MMC MODE. TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL

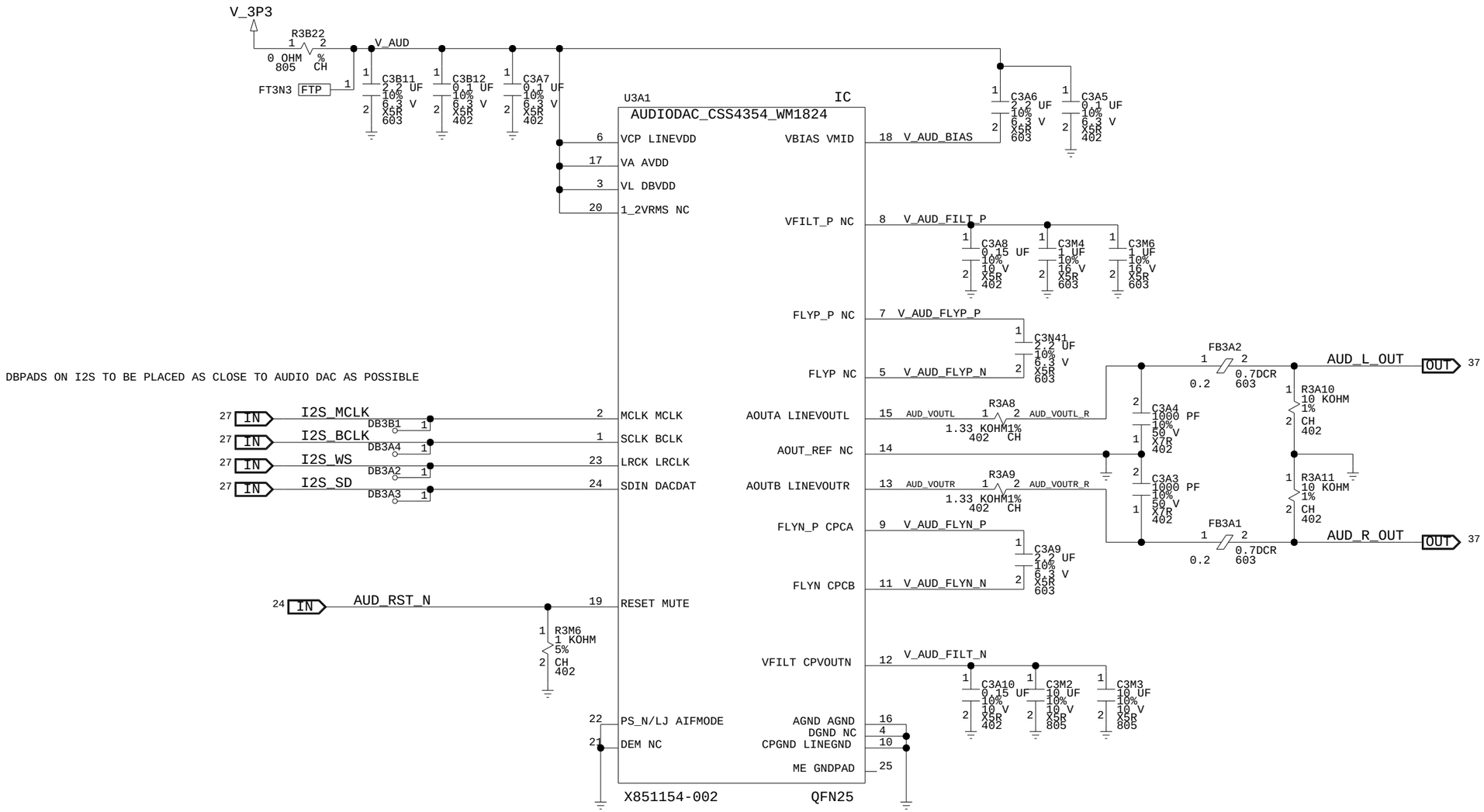


[PAGE_TITLE=MMC + FLASH]

DRAWING
Thu Feb 17 10:12:18 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	32/87	E	1.01

KSB OUT, AUDIO



[PAGE_TITLE=PSB OUT, AUDIO]

DRAWING
Thu Feb 17 10:12:20 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	33/87	E	1.01

KSB OUT, FLASH

ALL COMPONENTS ON THIS PAGE IS FOR MAMD MODE. TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL

N: STUFFED AT CONFIG LEVEL

V_3P3STBY

R2T13 10 KOHM 5% EMPTY 402

R2T12 10 KOHM 5% CH 402

R1D2 10 KOHM 5% CH 402

C1D1 4.7 UF 10% 6.3 V X5R 603

C1E17 0.1 UF 10% 6.3 V X5R 402

C2T18 0.1 UF 10% 6.3 V X5R 402

FT2T12 FTP
FT2T11 FTP
FT2T10 FTP
FT2T8 FTP
FT2T5 FTP
FT2T4 FTP
FT2T3 FTP
FT2T2 FTP

32 26 63 IN FLSH_DATA<7..0>

FTP FT1R1

R2T14 10 KOHM 5% CH 402
R2T11 10 KOHM 5% EMPTY 402
R2T10 10 KOHM 5% CH 402
R2T9 10 KOHM 5% CH 402
R2T7 10 KOHM 5% CH 402
R2T6 10 KOHM 5% CH 402
R2T2 10 KOHM 5% CH 402
R2T1 10 KOHM 5% CH 402

63 26 IN FLSH_WP_N

R1D1 10 KOHM 5% CH 402

U1E2 NAND FLASH

37	VCC1	
12	VCC0	
44	DATA<7>	
43	DATA<6>	
42	DATA<5>	
41	DATA<4>	
32	DATA<3>	
31	DATA<2>	
30	DATA<1>	
29	DATA<0>	
9	CE_N*	26 IN FLSH_CE_N
8	RE_N*	26 IN FLSH_RE_N
18	WE_N*	26 IN FLSH_WE_N
19	WP_N*	
17	ALE	26 IN FLSH_ALE
16	CLE	26 IN FLSH_CLE
6	VSS/NC	
36	VSS1	
13	VSS0	

X818098-001

I97 V_3P3STBY

I96 R2R1 2.2 KOHM 5% CH 402

IC

RDY 7 FLSH_READY OUT 26

FLSH_NC38 R2T8 0 OHM 5% 402 EMPTY

38	NC<27>
48	NC<26>
47	NC<25>
46	NC<24>
45	NC<23>
40	NC<22>
39	NC<21>
35	NC<20>
34	NC<19>
33	NC<18>
28	NC<17>
27	NC<16>
26	NC<15>
25	NC<14>
24	NC<13>
23	NC<12>
22	NC<11>
21	NC<10>
20	NC<9>
15	NC<8>
14	NC<7>
11	NC<6>
10	NC<5>
5	NC<4>
4	NC<3>
3	NC<2>
2	NC<1>
1	NC<0>

TSOP

NAND BOOTSTRAP FOR KSB

FLSH_DATA[1:0]	FLASH CONFIGURATION	
0X0	0.5KB, 16KB BLOCKS, 128MBIT	RETAIL
0X1	0.5KB, 16KB BLOCKS, 512MBIT	RETAIL
0X2	2KB PAGES, 128KB BLOCKS, 1/2/4 GBIT	XDK
0X3	4KB PAGES, 256KB BLOCKS, 2/4/8 GBIT	XDK

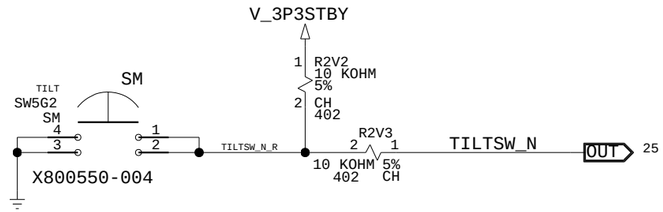
[PAGE_TITLE=PSB OUT, FLASH]

DRAWING
Thu Feb 17 10:12:25 2011

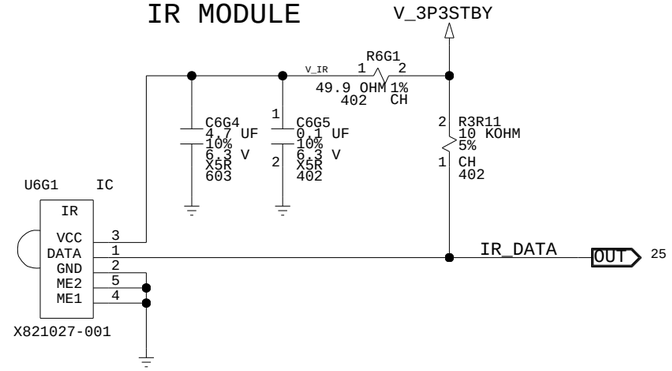
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	34/87	E	1.01

CONN, INFARED + SWITCHES + AUDIBLE F/B

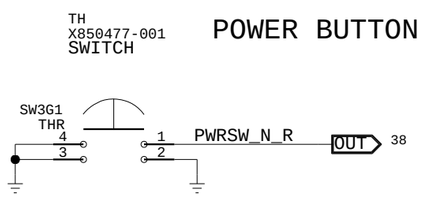
TILT SWITCH, SOLICO



IR MODULE



POWER BUTTON



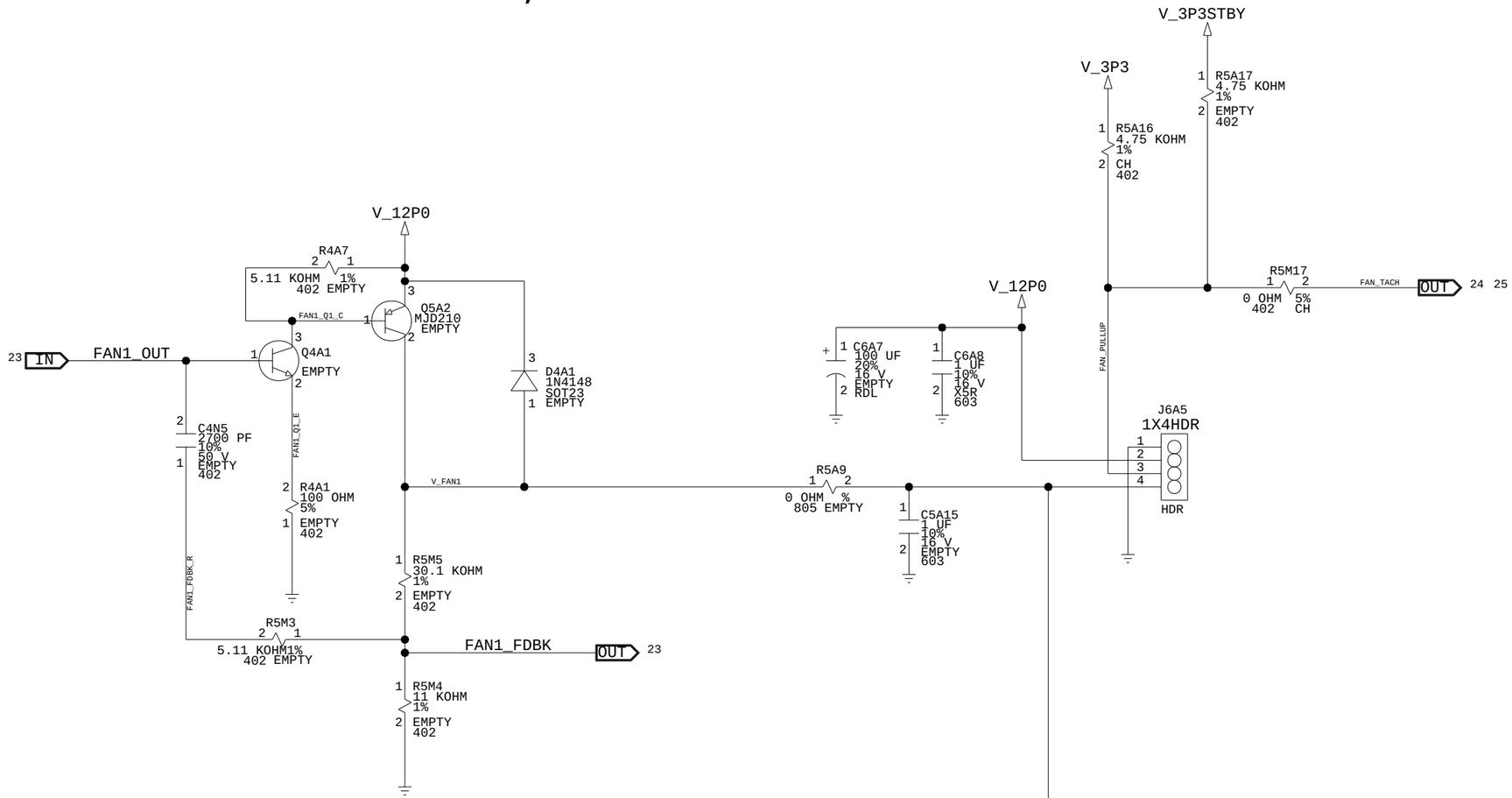
AUDIBLE FEEDBACK

[PAGE_TITLE=CONN,INFRARED+SWITCHES+AUDIBLE F/B]

DRAWING
Thu Feb 17 10:12:27 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	35/87	E	1.01

CONN, FAN



FAN CONTROL

[PAGE_TITLE= CONN, FAN]

DRAWING
Thu Feb 17 10:12:28 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	36/87	E	1.01

CONN, AVIP

DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS

V_5P0 — RT3A1 01.10 A THRMSTR 1206 — C2A8 4.7 UF 10% 6.3 V X5R 603 — C3A12 470 PF 5% 50 V X7R 402

V_AVIP — OUT 39 40

27 IN DBPAD ON SPDIF TO BE PLACED AS CLOSE TO CONN AS POSSIBLE — C3A13 22 PF 5% 50 V NPO 402 — EG3A6 X807267-001 ESDB-MLP7 DIO 402

J4A2 CONN — XENON AVIP CONNECTOR — X856166-001 TH

29	V_AVIP	
27	V_AVIP_RET	
37 IN	VID_DACA_OUT	4 VID_DACA_OUT, 2 VID_DACA_RET
37 IN	VID_DACB_OUT	3 VID_DACB_OUT, 1 VID_DACB_RET
37 IN	VID_DACC_OUT	8 VID_DACC_OUT, 6 VID_DACC_RET
37 IN	VID_DACD_OUT	7 VID_DACD_OUT, 5 VID_DACD_RET
37 IN	VID_HSYNC_OUT	11 VID_HSYNC_OUT, 9 VID_HSYNC_RET
37 IN	VID_VSYNC_OUT	12 VID_VSYNC_OUT, 10 VID_VSYNC_RET
	SPDIF_OUT (DB3A1)	25 SPDIF
33 IN	AUD_R_OUT	15 AUD_R_OUT, 13 AUD_R_RET
33 IN	AUD_L_OUT	16 AUD_L_OUT, 14 AUD_L_RET
		17 WSS_CNTL, 19 SCART_RGB
	EXT_PWR_ON	30 EXT_PWR_ON_N — OUT 62 63 25 37 64
	DDC_CLK	21 HDMI_DDC_CLK — BI 23 40 55
	DDC_DATA	23 HDMI_DDC_DATA — BI 23 40 55
	AV_MODE2	28 AV_MODE2 — OUT 25 37
	AV_MODE1	24 AV_MODE1 — OUT 25 37
	AV_MODE0	20 AV_MODE0 — OUT 25 37
	GND<2>	26
	GND<1>	22
	GND<0>	18
	SHIELD<3>	34
	SHIELD<2>	33
	SHIELD<1>	32
	SHIELD<0>	31
	MTGB<8-1>	
	MTGA<8-1>	

V_12P0 — R3A5 1.82 KOHM 1% CH 402

24 IN WSS_CNTL1 — R3A3 5.36 KOHM 1% 402 CH

24 IN WSS_CNTL0 — R3A4 4.75 KOHM 1% 402 CH

Q3A1 XSTR — WSS_CNTL_B — WSS_CNTL_E — WSS_CNTL_OUT_R — WSS_CNTL_OUT

R3A6 301 OHM 1% 603 CH — R3A1 10 KOHM 1% 402 CH — R3A2 1 KOHM 5% 402 CH

C3A1 75 PF 5% 50 V NPO 402

V_3P3 — Q3M1 XSTR — SCART_RGB_OUT

24 IN SCART_RGB — R2M2 10 KOHM 5% 402 CH — SCART_RGB_R — R3M7 33 OHM 5% 402 CH — SCART_RGB_OUT_R — R3M2 10 KOHM 5% 402 CH — C3M1 0.01 UF 10% 16 V X7R 402

V_3P3STBY

63 62 37 IN EXT_PWR_ON_N — R3P5 10 KOHM 5% 2 CH 402

37 IN AV_MODE2 — R2N1 10 KOHM 5% 2 CH 402

37 IN AV_MODE1 — R3N6 10 KOHM 5% 2 CH 402

37 IN AV_MODE0 — R2C3 10 KOHM 5% 2 CH 402

C3A2 470 PF 5% 50 V X7R 402 — C2M2 470 PF 5% 50 V X7R 402 — C2M1 470 PF 5% 50 V X7R 402 — C2C2 470 PF 5% 50 V X7R 402

LAYOUT:PLACE CLOSE TO CONNECTOR EMI CAPS

23 IN VID_VSYNC_OUT_R — R3C25 49.9 OHM 1% 402 CH — VID_VSYNC_OUT — OUT 37 — EG4A9 X807267-001 ESDB-MLP7 DIO 402

23 IN VID_HSYNC_OUT_R — R3C24 49.9 OHM 1% 402 CH — VID_HSYNC_OUT — OUT 37 — EG4A10 X807267-001 ESDB-MLP7 DIO 402

VID_DACA_DP — R4A11 4.75 OHM 1% 402 CH — VID_DACA_DP_L — R4A5 75 OHM 1% CH 402 — EG4A8 X807267-001 ESDB-MLP7 DIO 402 — V_1P2 — U4M1 BAV99 DIO — L4A4 .27 UH 0.45 A 360 IND 1210 — VID_DACA_OUT — C4A10 62 PF 5% 50 V NPO 402 — C4A3 33 PF 5% 50 V NPO 402 — V_1P2 — U4A2 BAV99 DIO — OUT 37

VID_DACC_DP — R4A12 4.75 OHM 1% 402 CH — VID_DACC_DP_L — R4A3 75 OHM 1% CH 402 — EG4A6 X807267-001 ESDB-MLP7 DIO 402 — V_1P2 — U4M1 BAV99 DIO — L4A2 .27 UH 0.45 A 360 IND 1210 — VID_DACC_OUT — C4A8 62 PF 5% 50 V NPO 402 — C4A5 33 PF 5% 50 V NPO 402 — V_1P2 — U4A2 BAV99 DIO — OUT 37

VID_DACB_DP — R4A10 4.75 OHM 1% 402 CH — VID_DACB_DP_L — R4A4 75 OHM 1% CH 402 — EG4A7 X807267-001 ESDB-MLP7 DIO 402 — V_1P2 — U4M2 BAV99 DIO — L4A3 .27 UH 0.45 A 360 IND 1210 — VID_DACB_OUT — C4A9 62 PF 5% 50 V NPO 402 — C4A6 33 PF 5% 50 V NPO 402 — V_1P2 — U4A1 BAV99 DIO — OUT 37

VID_DACD_DP — R4A9 4.75 OHM 1% 402 CH — VID_DACD_DP_L — R4A2 75 OHM 1% CH 402 — EG4A5 X807267-001 ESDB-MLP7 DIO 402 — V_1P2 — U4M2 BAV99 DIO — L4A1 .27 UH 0.45 A 360 IND 1210 — VID_DACD_OUT — C4A7 62 PF 5% 50 V NPO 402 — C4A4 33 PF 5% 50 V NPO 402 — V_1P2 — U4A1 BAV99 DIO — OUT 37

V_1P2 — C4M3 0.1 UF 10% 25 V X5R 402 — C4M2 0.1 UF 10% 25 V X5R 402

DECOUPLING FOR BAV99DW

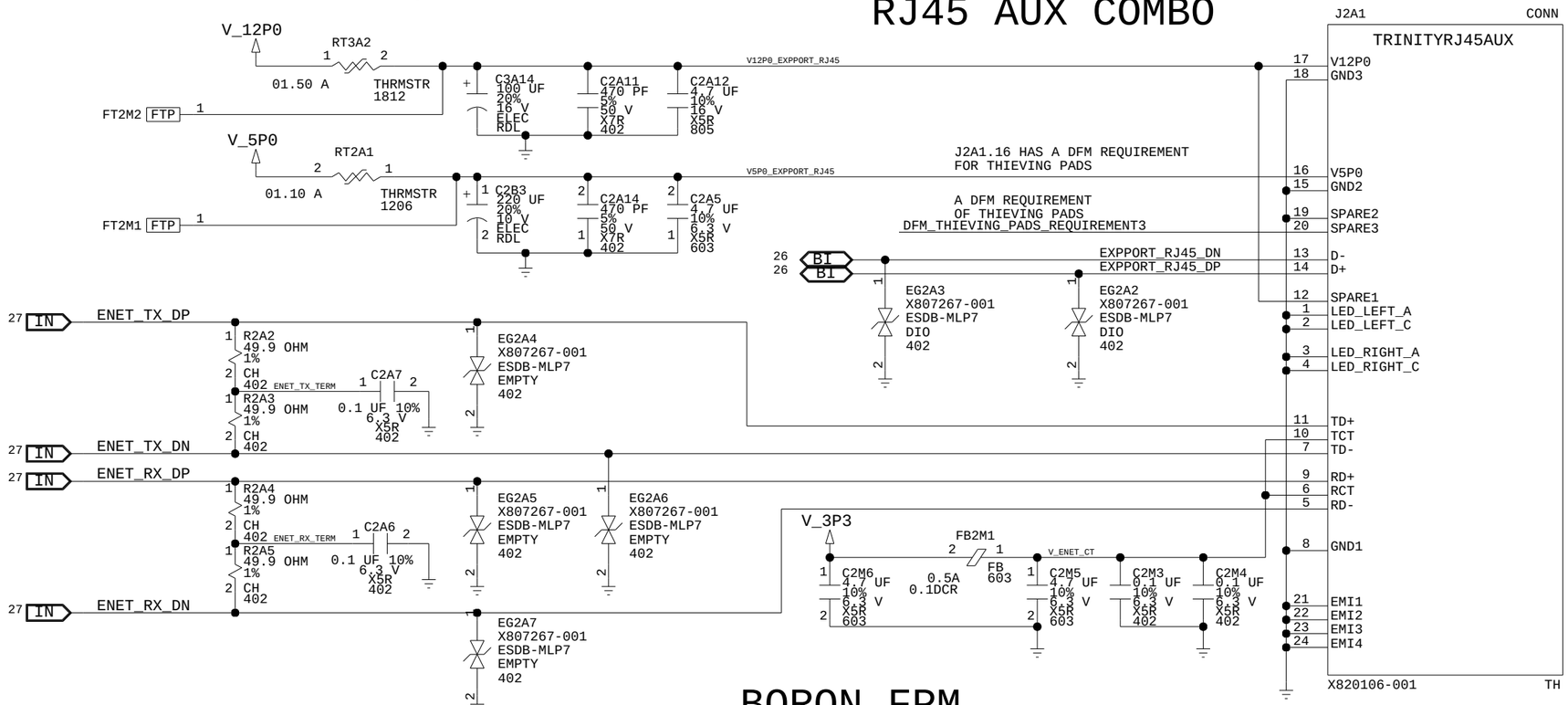
[PAGE_TITLE=[CONN, AVIP]

DRAWING Thu Feb 17 10:12:28 2011

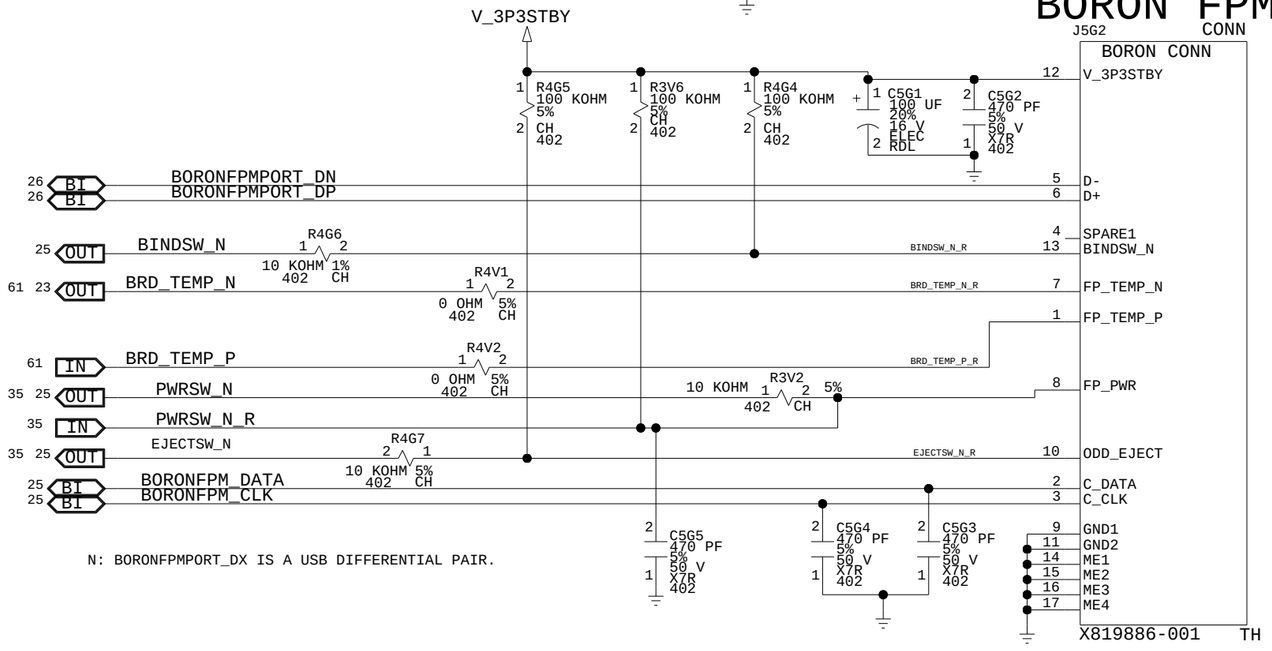
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	37/87	E	1.01

CONN, RJ45 USB AUX COMBO + BORON + PWR

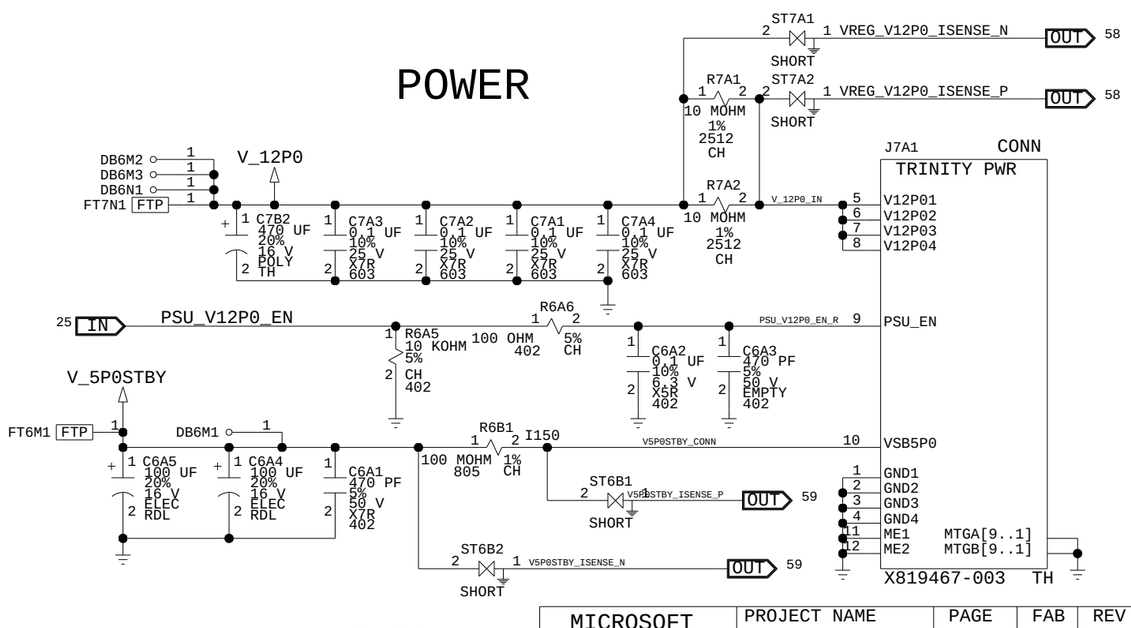
RJ45 AUX COMBO



BORON FPM



POWER



[PAGE_TITLE=CONN, RJ45 AUX COMBO + BORON + PWR]

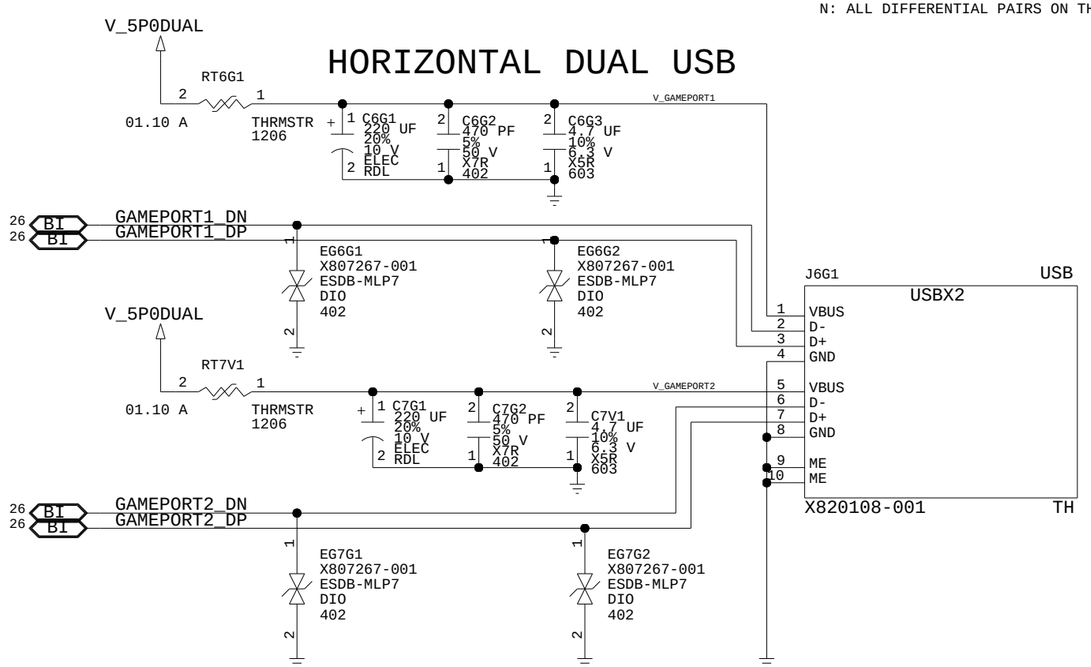
DRAWING
Thu Feb 17 10:12:28 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	38/87	E	1.01

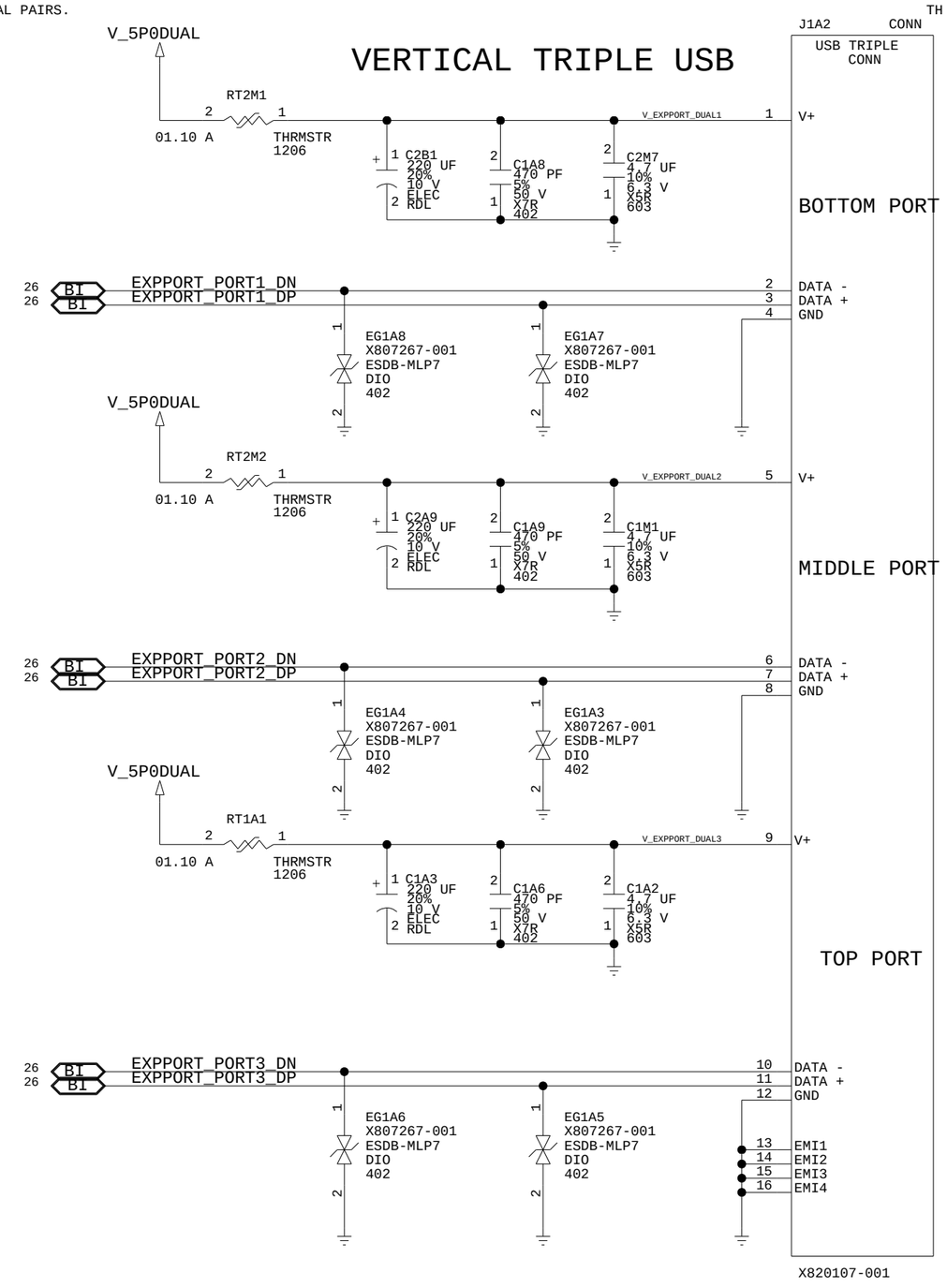
CONN, USB + MEM PORTS + TOSLINK + WAVEPORT

N: ALL DIFFERENTIAL PAIRS ON THIS PAGE ARE USB DIFFERENTIAL PAIRS.

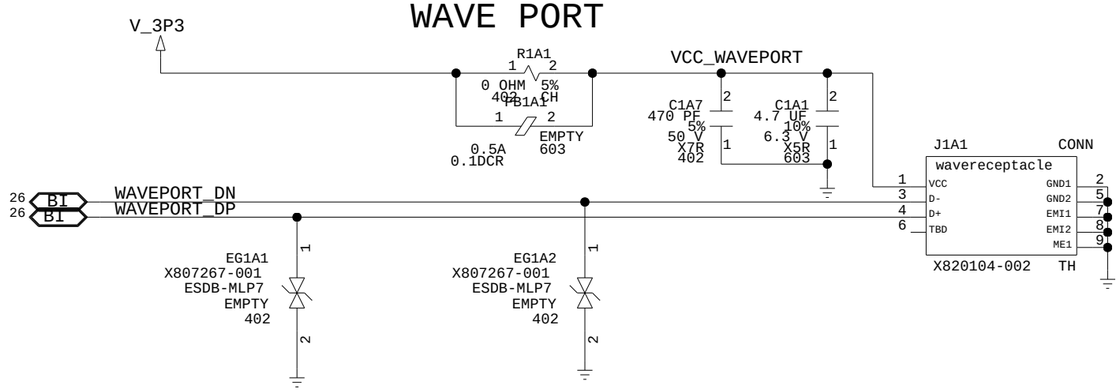
HORIZONTAL DUAL USB



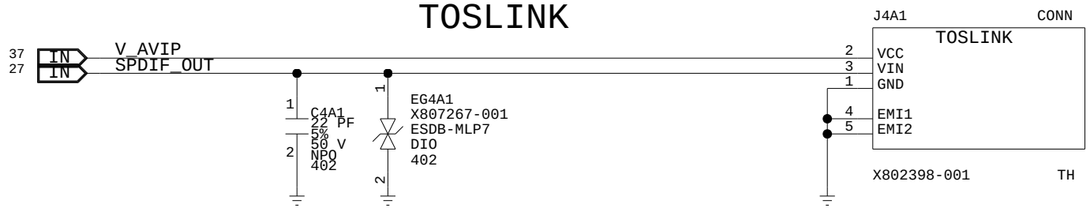
VERTICAL TRIPLE USB



WAVE PORT



TOSLINK



[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING
Thu Feb 17 10:12:28 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	39/87	E	1.01

CONN, HDMI

FT3M7 FTP 1
FT3M1 FTP 1
23 IN HDMI_TX2_DP
23 IN HDMI_TX2_DN
FT3M2 FTP 1
FT3M8 FTP 1
EG3A2 X807267-001 ESDB-MLP7 DIO 402
EG3A1 X807267-001 ESDB-MLP7 DIO 402

FT3M9 FTP 1
FT3M3 FTP 1
23 IN HDMI_TX1_DP
23 IN HDMI_TX1_DN
FT3M4 FTP 1
FT3M10 FTP 1
EG3A4 X807267-001 ESDB-MLP7 DIO 402
EG3A3 X807267-001 ESDB-MLP7 DIO 402

FT3M11 FTP 1
FT3M5 FTP 1
23 IN HDMI_TX0_DP
23 IN HDMI_TX0_DN
FT4M2 FTP 1
FT4M7 FTP 1
EG4A2 X807267-001 ESDB-MLP7 DIO 402
EG3A5 X807267-001 ESDB-MLP7 DIO 402

FT4M8 FTP 1
FT4M3 FTP 1
23 IN HDMI_TXC_DP
23 IN HDMI_TXC_DN
FT4M4 FTP 1
FT4M9 FTP 1
EG4A4 X807267-001 ESDB-MLP7 DIO 402
EG4A3 X807267-001 ESDB-MLP7 DIO 402

V_5P0STBY
R4M2 2 KOHM 1% 2 CH 402
R4M1 2 KOHM 1% 2 CH 402
FT4M5 FTP 1
37 23 IN HDMI_DDC_CLK
55 37 23 BI HDMI_DDC_DATA
FT4M1 FTP 1
EG4M2 X807267-001 ESDB-MLP7 DIO 402
EG4M1 X807267-001 ESDB-MLP7 DIO 402

37 IN V_AVIP
C3A11 0.1 UF 10% 6.3 V X5R 402

J3A1 HDR
HDMI
1 TMDS_DATA2_DP
2 TMDS_DATA2_SHD
3 TMDS_DATA2_DN
4 TMDS_DATA1_DP
5 TMDS_DATA1_SHD
6 TMDS_DATA1_DN
7 TMDS_DATA0_DP
8 TMDS_DATA0_SHD
9 TMDS_DATA0_DN
10 TMDS_CLK_DP
11 TMDS_CLK_SHD
12 TMDS_CLK_DN
13 CEC
14 RESERVED
15 SCL
16 SDA
17 DDC_CEC_GND
18 5VCC
19 HOT_PLUG_DET
23 ME4
22 ME3
21 ME2
20 ME1
X806395-002

DB3M1 1 HDMI_CEC

HDMI_HPD_PIN
R4M6 10 KOHM 5% 402 CH
1 FTP FT4M6
HDMI_HPD OUT 23
R4M5 47.5 KOHM 1% 2 CH 402
EG4M5 X807267-001 ESDB-MLP7 DIO 402

[PAGE_TITLE=CONN, HDMI]

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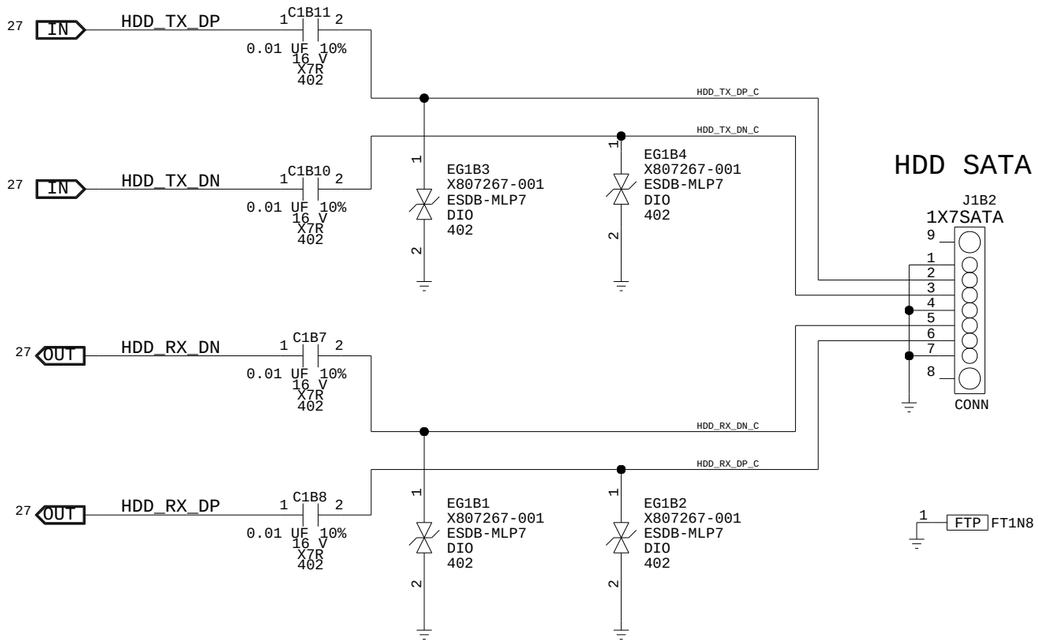
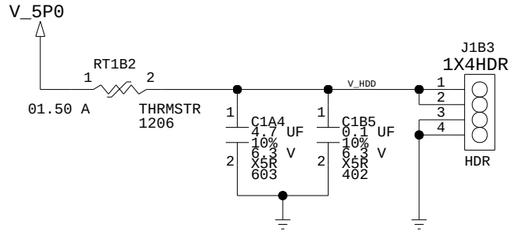
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	40/87	E	1.01

CONN, ODD + HDD

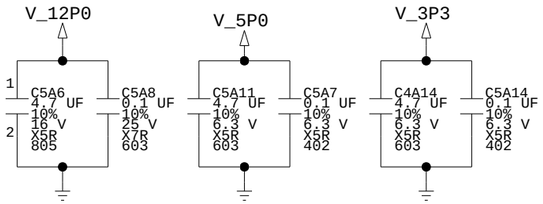
HDD SATA



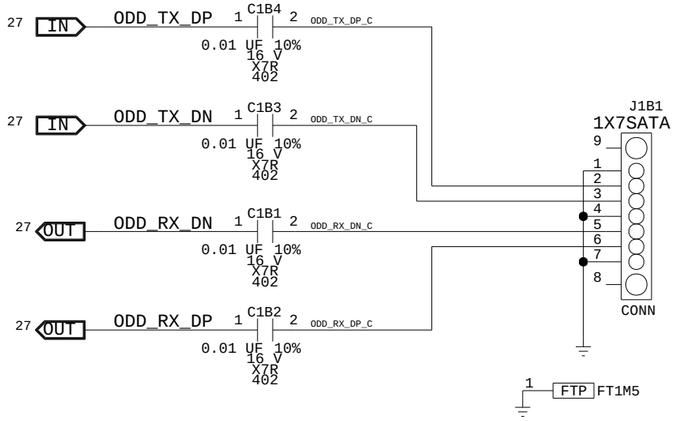
HDD POWER



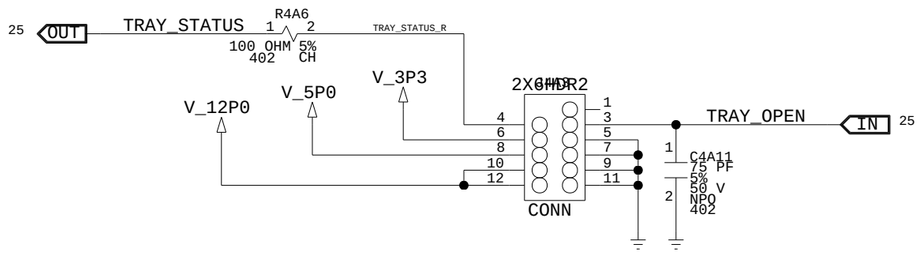
ODD POWER DECOUPLING



ODD SATA



ODD POWER AND CONTROL



[PAGE_TITLE=CONN, ODD + HDD + MU]

DRAWING
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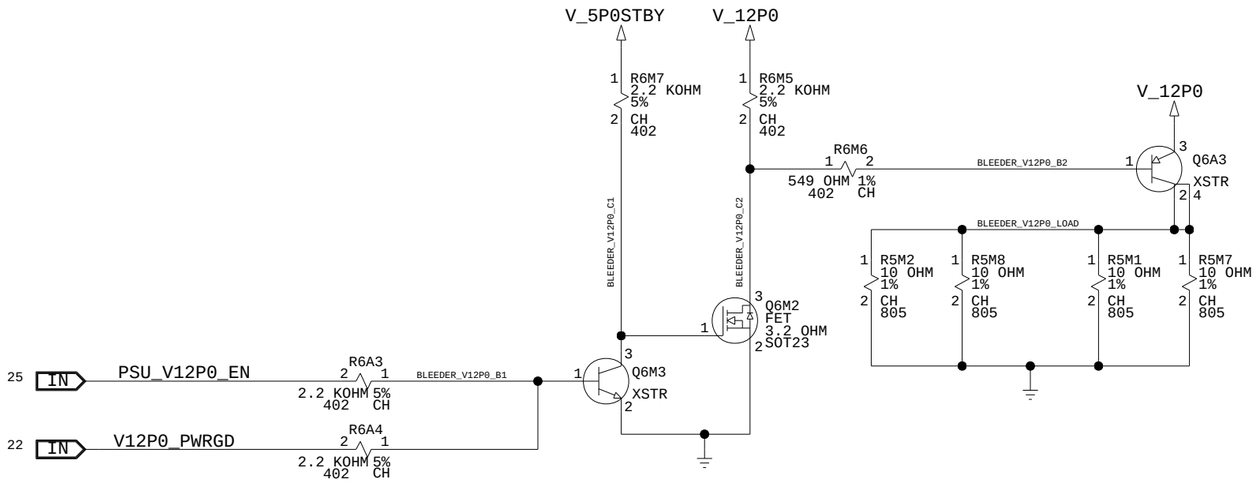
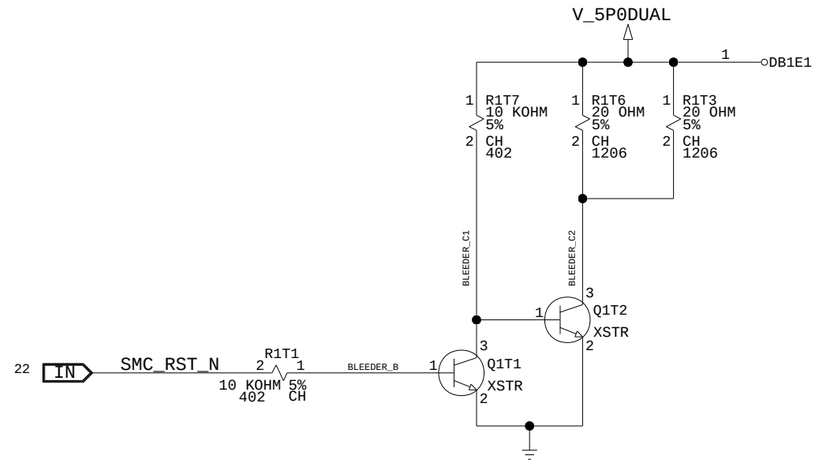
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	41/87	E	1.01

VREG, BLEEDERS



V_12P0 & V_5P0 BLEEDERS



V_5P0DUAL BLEEDER

[PAGE_TITLE= VREGS,_BLEEDERS]

DRAWING
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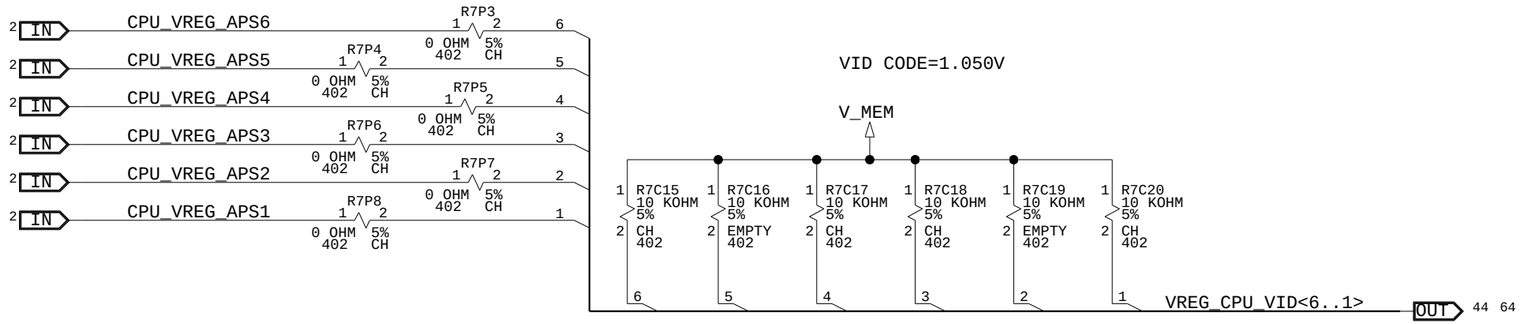
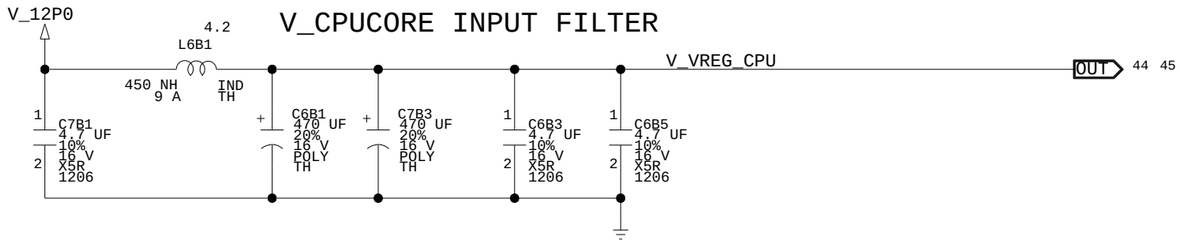
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	42/87	E	1.01

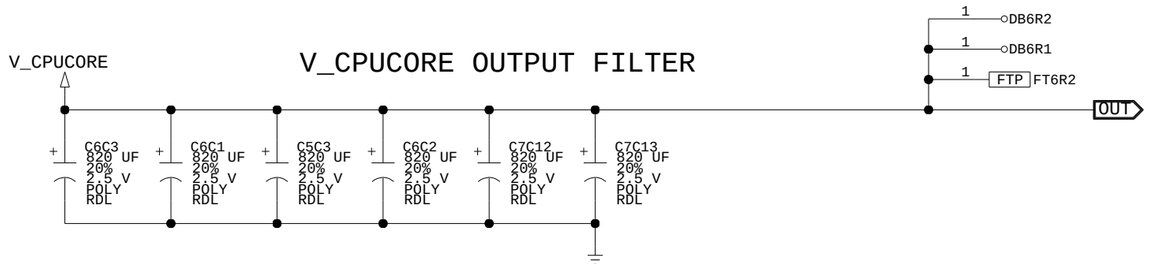
VREGS, INPUT + OUTPUT FILTERS



V_CPUCORE INPUT FILTER



V_CPUCORE OUTPUT FILTER



[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

DRAWING
Thu Feb 17 10:12:29 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	43/87	E	1.01

VREGS, CPU CONTROLLER

43 IN V_VREG_CPU
25 IN VREG_CPU_EN
FT3P8 FTP
R7C10 10 KOHM 5% CH 402
R7C11 681 OHM 1% 603 CH
R7C12 681 OHM 1% 603 CH
R7B5 1 KOHM 5% 402 CH
RRAMP VREG_CPU_RAMPADJ_R
C7P2 0.1 UF 10% 25 V X7R 603
R7C4 422 KOHM 1% 402 CH
C7C10 4.7 UF 10% 16 V X5R 1206
C7C11 1 UF 10% 16 V X5R 603
VREG_CPU_VCC OUT 44
VREG_CPU_VCC3_3P3
C7C9 0.1 UF 10% 6.3 V X5R 402
R7C13 10 KOHM 5% CH 402
U7C1 NCP4201 IC
X817912-001
VREG_CPUCORE_PWRGD OUT 25
VREG_CPU_VID<6..1> IN 43
VID'S HAVE INTERNAL PULL DOWNS
VREG_CPU_RAMPADJ 11
55 IN PMBUS_CLK
60 59 58 57 56 55 64 BI PMBUS_DATA
45 IN VREG_CPU_PHASE2
45 IN VREG_CPU_PHASE1
64 OUT VREG_CPU_CSCOMP
64 OUT VREG_CPU_CSSUM
64 OUT VREG_CPU_CSREF
R7C7 0 OHM 5% 402 CH
R7C9 0 OHM 5% 402 CH
DB7C2 VREG_CPU_SW4
DB7C3 VREG_CPU_SW3
VREG_CPU_PHASE2_R
VREG_CPU_PHASE1_R
VREG_CPU_VCC OUT 44
VREG_CPU_PWM2 OUT 45
VREG_CPU_PWM1 OUT 45
VREG_CPU_DRV_EN OUT 45
VREG_CPU_OD1_N
DB7C1
DB7P1
DB7P2
VREG_CPU_ALERT_N
VREG_CPU_FAULT_N
VREG_CPU_IMON
VREG_CPU_RT
R7C5 909 KOHM 1% CH 402
ROSC = 909K
FOSC = 250KHZ
RTH1 R6C2 603 THRMSTR TEMP SENSOR
RCS2 R7B1 35.7 KOHM 1% 402 CH
RCS1 R7B2 52.3 KOHM 1% CH 402
RPH2 R7B3 27.4 KOHM 1% CH 402
RPH1 R7B4 27.4 KOHM 1% CH 402
CCS2 C7C1 3300 PF 10% 50 V X7R 402
CCS1 C7C3 3300 PF 10% 50 V X7R 402
VREG_CPU_CSCOMP_R
R7C1 6.81 KOHM 1% 402 CH
NEED TO SET DURING VALIDATION
R7C6 121 KOHM 1% CH 402
VREG_CPU_FB
VREG_CPU_COMP
VREG_CPU_FBRTN
VREG_CPU_TRDET
VREG_CPU_IREF
VREG_CPU_ILIMITFS
PARTS ARE TRIMMED AT FACTORY SUCH THAT VBOOT=1.05V

I2C ADDRESS			
	1100 000	R/W	HEX
WRITE	1100 000	0	0XC0
READ	1100 000	1	0XC1

V_CPUCORE
PLACE SHORT NEXT TO OUTPUT OF DUAL INDUCTOR
ST6C1 SHORT
VENABLE
ST6D1 SHORT
VREG_V_CPUCORE_S
R7C14 0 OHM % 805 EMPTY
DB7C5
DB7C6
PLACE SHORT NEXT TO POINT OF LOAD
CB C7C2 470 PF 5% 50 V X7R 402
RB R7P1 1.1 KOHM 1% 402 CH
CA C7C5 1500 PF 10% 50 V X7R 402
RA R7P2 18.2 KOHM 1% 402 CH
C7P1 1000 PF 10% 50 V X7R 402
CFB C7C4 10 PF 5% 50 V NPO 402
ST6D2 SHORT
PLACE SHORT NEXT TO POINT OF LOAD
R7C2 43.2 KOHM 1% 402 CH
R7C3 10 KOHM 5% 402 CH
C7B7 470 PF 5% 50 V X7R 402
C7C7 0.1 UF 10% 6.3 V X5R 402
R7C8 5.76 KOHM 1% CH 402
NOTE: VALID UP TO 58A
C7C6 1000 PF 10% 50 V X7R 402

[PAGE_TITLE=VREGS, CPU CONTROLLER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	44/87	E	1.01

VREG, CPU OUTPUT PHASE 1 & 2

43 IN V_VREG_CPU

R6N1 2.2 OHM 1% 805 CH — VREG_CPU2_VCC — C6B4 1 UF 10% 16 V X5R 603

D6B1 1N4148 SOT23 DIO

VREG_CPU_BST2 — C6N1 0.01 UF 10% 50 V EMPTY 805

R6N2 2.2 OHM 1% 805 CH — VREG_CPU_BST2_R — C6N2 0.1 UF 10% 25 V X7R 603

U6B1 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

VREG_CPU_DRVH2

Q6B2 7.5 MOHM DPAK_G1D2S3 FET

C7B5 4.7 UF 10% 16 V X5R 1206

C7N1 4.7 UF 10% 16 V EMPTY 1206

44 IN VREG_CPU_PWM2

44 IN VREG_CPU_DRV_EN

VREG_CPU_DRVL2

Q6C2 X819087-001 DPAK_G1D2S3 FET

Q6C1 X819087-001 DPAK_G1D2S3 FET

R6C1 1 OHM 1% CH 805 — VREG_CPU_SW2_R — C7C8 2200 PF 10% 50 V X7R 805

VREG_CPU_PHASE2 OUT 44

V_CPUCORE
NOM.VOLTAGE: 0.9-1.2V

V_CPUCORE

L6C1 SM EMPTY DUAL INDUCTOR (L1, L4, L3, L2) — X820048-001 420NH

DCR +/-8%

DB7C4

V_CPUCORE

L6C2 IND DUAL INDUCTOR (L2, L3, L4, L1) — X850592-001 420NH 40 A 0.66 +/-4%

NOTE: THRUHOLE PART IS 2% IMPROVEMENT ON DCR

R5N7 2.2 OHM 1% 805 CH — VREG_CPU1_VCC — C5B10 1 UF 10% 16 V X5R 603

D5B1 1N4148 SOT23 DIO

VREG_CPU_BST1 — C5N5 0.01 UF 10% 50 V EMPTY 805

R5N8 2.2 OHM 1% 805 CH — VREG_CPU_BST1_R — C5N6 0.1 UF 10% 25 V X7R 603

U5B5 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

VREG_CPU_DRVH1

Q6B1 7.5 MOHM DPAK_G1D2S3 FET

C6B2 4.7 UF 10% 16 V X5R 1206

C6N3 4.7 UF 10% 16 V EMPTY 1206

44 IN VREG_CPU_PWM1

VREG_CPU_DRVL1

Q5C3 X819087-001 DPAK_G1D2S3 FET

Q5C1 X819087-001 DPAK_G1D2S3 FET

VREG_CPU_PHASE1 OUT 44

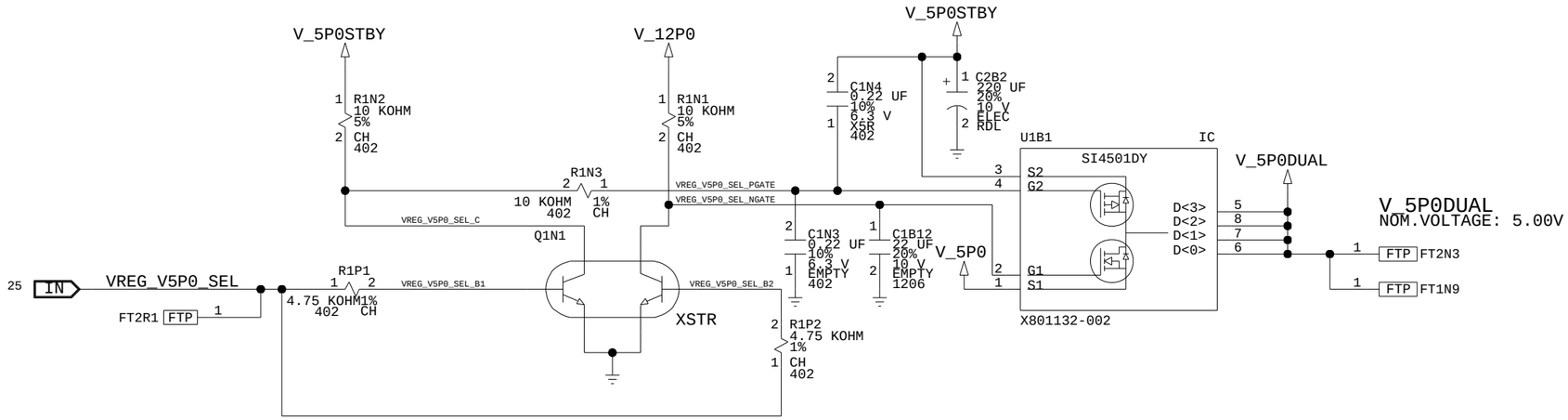
R5C1 1 OHM 1% CH 805 — VREG_CPU_SW1_R — C5C1 2200 PF 10% 50 V X7R 805

[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2]

DRAWING
Thu Feb 17 10:12:30 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	45/87	E	1.01

VREGS, V5P0 DUAL



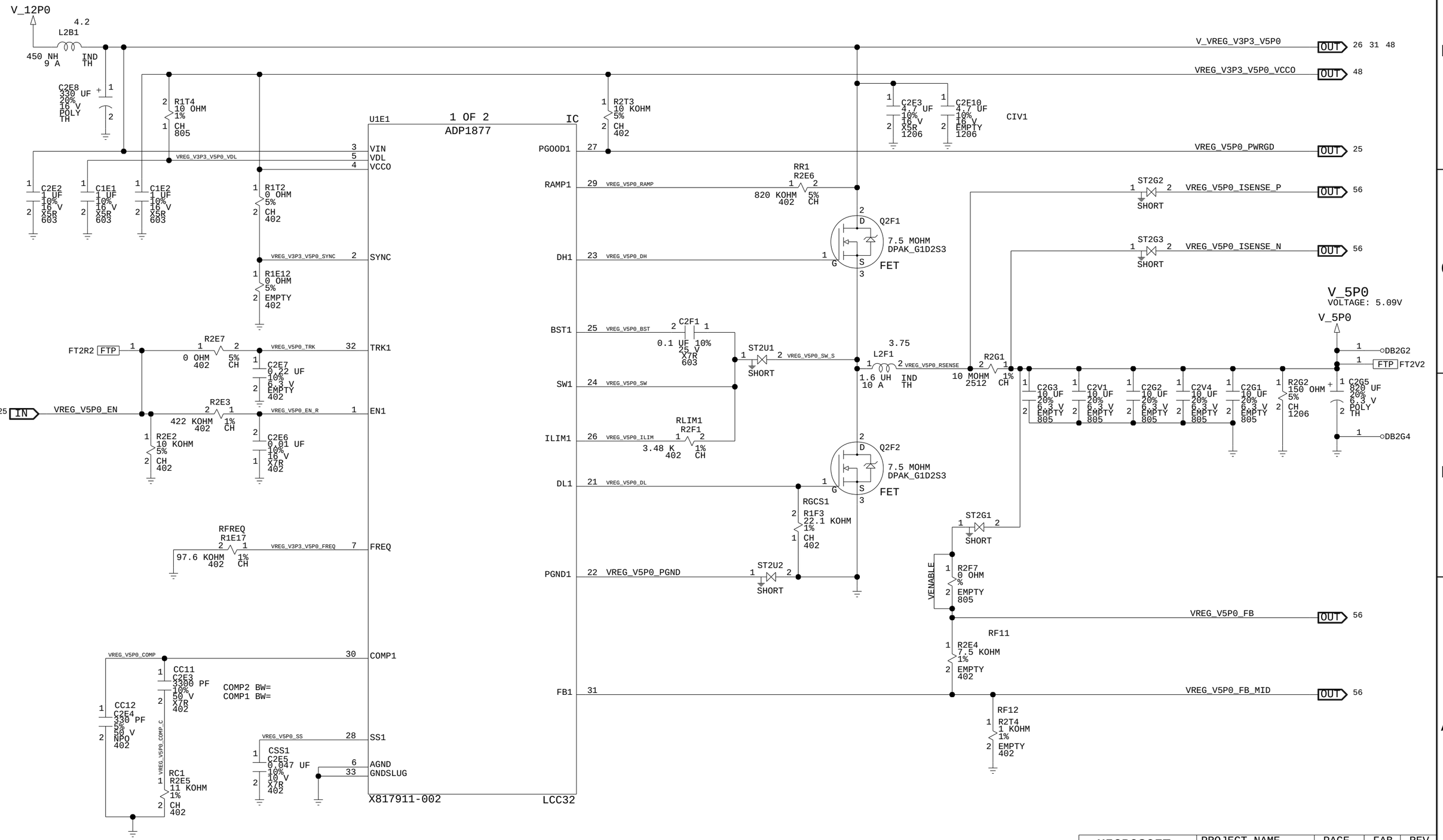
VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=VREGS, V5P0 DUAL]

DRAWING
Thu Feb 17 10:12:30 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	46/87	E	1.01

VREGS, V5P0



[PAGE_TITLE=VREGS, V5P0]

DRAWING
Thu Feb 17 10:12:30 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	47/87	E	1.01

VREGS, V3P3

47 IN V_VREG_V3P3_V5P0
47 IN VREG_V3P3_V5P0_VCCO

U1E1 2 OF 2 ADP1877 IC

R1E14 10 KOHM 5% CH 402

PGOOD2 14 → VREG_V3P3_PWRGD OUT 25

RAMP2 12 VREG_V3P3_RAMP — R1E22 422 KOHM 1% 402 CH

DH2 18 VREG_V3P3_DH

BST2 16 VREG_V3P3_BST — C1F1 0.1 UF 10% 25 V X7R 603 — ST1E1 SHORT

SW2 17 VREG_V3P3_SW

ILIM2 15 VREG_V3P3_ILIM — R1F1 4.53 KOHM 1% 402 CH

DL2 20 VREG_V3P3_DL — R1F2 22.1 KOHM 1% 402 CH

PGND2 19 VREG_V3P3_PGND — ST1U1 SHORT

FB2 10

COMP2 11

SS2 13

X817911-002

LCC32

R1E15 0 OHM 5% 402 CH — VREG_V3P3_TRK 9 TRK2

FT3R4 FTP 1

25 IN VREG_V3P3_EN — 8 EN2

R1E16 10 KOHM 5% 2 CH 402

VREG_V3P3_COMP — C1E3 3300 PF 10% 50 V X7R 402 — C1E4 120 PF 5% 50 V NPO 402 — VREG_V3P3_COMP_C — R1E21 7.87 KOHM 1% 2 CH 402

VREG_V3P3_SS — C1E5 0.047 UF 10% 10 V X7R 402

U1F1 7 AMP FET — GATE0 SRC0 GATE1 SRC1 DRN0 DRN0 DRN1 DRN1 — X807111-001 SO-8

C1U1 4.7 UF 10% 16 V X5R 1206

VREG_V3P3_SW_S — L1F1 0.02 2.3 UH 6 A IND SM — VREG_V3P3_RSENSE

R1F9 30 MOHM 2512 CH 1%

ST1F1 SHORT — VREG_V3P3_ISENSE_P OUT 56

ST1F3 SHORT — VREG_V3P3_ISENSE_N OUT 56

V_3P3 V_3P3 VOLTAGE: 3.3V

FT2U1 — DB2G1 — DB2F1

C1F9 4.7 UF 10% 6.3 V X5R 603
C1E6 4.7 UF 10% 6.3 V X5R 603
C1G2 4.7 UF 10% 6.3 V X5R 603
C1F3 4.7 UF 10% 6.3 V X5R 603

VENABLE — R2F9 0 OHM % 805 EMPTY — ST1F2 SHORT

VREG_V3P3_FB OUT 56

R1E20 4.53 KOHM 1% EMPTY 402

VREG_V3P3_FB_MID OUT 56

R1E19 1 KOHM 1% EMPTY 402

[PAGE_TITLE=VREGS, V3P3]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	48/87	E	1.01

VREGS, VEDRAM

V_12P0
L7B1 4.2
450 NH 9 A IND TH
C3F8 330 UF 20% 16 V POLY TH
C7B8 470 UF 20% 16 V POLY TH
R3G2 10 OHM 1% CH 805
U3G1 1 OF 2 ADP1877 IC
R3G16 10 KOHM 5% CH 402
C3F1 4.7 UF 10% 16 V X5R 1206
C3F7 4.7 UF 10% 16 V EMPTY 1206 CIV1
V_VREG_VMEM_VEDRAM OUT 50
VREG_VMEM_VEDRAM_VCCO OUT 50
VREG_VEDRAM_PWRGD OUT 25
C3G1 1 UF 10% 16 V X5R 603
C3G3 1 UF 10% 16 V X5R 603
C3V1 1 UF 10% 16 V X5R 603
SYNC HIGH=FORCED PWM MODE
SYNC LOW =PULSE SKIP MODE
R3F12 0 OHM 5% CH 402
R3F14 0 OHM 5% CH 402
R3F13 0 OHM 5% EMPTY 402
VREG_VMEM_VEDRAM_VDL
VREG_VMEM_VEDRAM_SYNC
VREG_VEDRAM_TRK
VIN 3
VDL 5
VCCO 4
SYNC 2
TRK1 32
PGOOD1 27
RAMP1 29 VREG_VEDRAM_RAMP
RR1 R3F10 680 KOHM 402 5% CH
DH1 23 VREG_VEDRAM_DH
Q3F1 7.5 MOHM DPAK_G1D2S3 FET
ST4F2 SHORT
VREG_VEDRAM_ISENSE_P OUT 55
ST4F4 SHORT
VREG_VEDRAM_ISENSE_N OUT 55
V_CPUEDRAM
V_CPUEDRAM VOLTAGE: 1.075V
3.4
L4F1 1.7 UH 13.8 A IND TH
VREG_VEDRAM_RSENSE
R4F1 10 MOHM 2512 1%
FTP FT4T2
DB4E3
BST1 25 VREG_VEDRAM_BST
C3F5 0.1 UF 10% 25 V X7R 603
ST3F1 SHORT
VREG_VEDRAM_SW_S
C4E3 820 UF 20% 2.5 V POLY RDL
C4E6 820 UF 20% 2.5 V POLY RDL
C4F7 820 UF 20% 2.5 V EMPTY RDL
SW1 24 VREG_VEDRAM_SW
RLIM1 R3F7 3.32 KOHM 402 1% CH
ILIM1 26 VREG_VEDRAM_ILIM
C5T52 4.7 UF 10% 16 V EMPTY 1206
C5E11 4.7 UF 10% 16 V EMPTY 1206
C4I7 4.7 UF 10% 16 V EMPTY 1206
C5E10 4.7 UF 10% 16 V EMPTY 1206
Q4F1 7.5 MOHM DPAK_G1D2S3 FET
DL1 21 VREG_VEDRAM_DL
RGCS1 R3V1 22.1 KOHM 1% CH 402
ST5E1 SHORT
DB4E4
DB4E5
VENABLE
R3F11 0 OHM 5% EMPTY 805
PGND1 22 VREG_VEDRAM_PGND
ST4U1 SHORT
VREG_VEDRAM_FB OUT 55
RF11 R3F8 7.87 KOHM 1% EMPTY 402
FB1 31
VREG_VEDRAM_FB_MID OUT 55
RF12 R3F9 10 KOHM 1% EMPTY 402
FT2T9 FTP
25 IN VREG_VEDRAM_EN
R3F15 10 KOHM 5% CH 402
EN1 1
RFREQ R3G4 97.6 KOHM 402 1% CH
VREG_VEDRAM_FREQ
FREQ 7
VREG_VEDRAM_COMP
COMP1 30
CC11 C3F2 4700 PF 10% 50 V X7R 402
CC12 C3F3 62 PF 5% 50 V NPO 402
VREG_VEDRAM_COMP_C
RC1 R3F6 43.2 KOHM 1% CH 402
RC1=120K
VREG_VEDRAM_SS
SS1 28
CSS1 C3F4 0.047 UF 10% 10 V X7R 402
AGND 6
GNDSLUG 33
X817911-002
LCC32

[PAGE_TITLE=[VREGS, VEDRAM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	49/87	E	1.01

VREGS, VMEM

49 IN V_VREG_VMEM_VEDRAM
49 IN VREG_VMEM_VEDRAM_VCCO

U3G1 2 OF 2 IC
ADP1877

R3G15 10 KOHM 5% CH 402

CIV2 C7F3 4.7 UF 10% 16 V X5R 1206
C7U1 4.7 UF 10% 16 V EMPTY 1206

PGOOD2 14 VREG_VMEM_PWRGD OUT 25

RAMP2 12 VREG_VMEM_RAMP
RR2 R3G13 680 KOHM 5% 402 CH

ST7F2 SHORT VREG_VMEM_ISENSE_P OUT 55
ST7F3 SHORT VREG_VMEM_ISENSE_N OUT 55

V_MEM
VOLTAGE: 1.8V

DH2 18 VREG_VMEM_DH
Q7G1 7.5 MOHM DPAK_G1D2S3 FET

R3G5 0 OHM 5% 402 CH
VREG_VMEM_TRK 9 TRK2

DB7F1
FTP FT7U1
V_MEM

FT2T1 FTP 1
25 IN VREG_VMEM_EN 8 EN2
R3G14 10 KOHM 5% CH 402

BST2 16 VREG_VMEM_BST
C3G9 0.1 UF 10% 25 V X7R 603
ST6V2 SHORT
VREG_VMEM_SW_S
L7F1 IND TH 1.7 UH 13.8 A 3.4
VREG_VMEM_RSENSE
R7F1 10 MOHM 1% 2512 CH

C7F2 820 UF 20% 2.5 V POLY RDL
C7F1 4.7 UF 10% 6.3 V EMPTY 603
DB7F2

V_MEM
C7R1 330 UF 20% 2.5 V EMPTY SM

V_MEM
C4U4 330 UF 20% 2.5 V EMPTY SM

SW2 17 VREG_VMEM_SW

ILIM2 15 VREG_VMEM_ILIM
RLIM2 R3G10 3.32 KOHM 1% 402 CH

DL2 20 VREG_VMEM_DL
Q7G2 7.5 MOHM DPAK_G1D2S3 FET

RGCS2 R4G3 22.1 KOHM 1% CH 402

PGND2 19 VREG_VMEM_PGND
ST6V1 SHORT

ST7F1 SHORT
VENABLE R3G17 0 OHM EMPTY 805

VREG_VMEM_FB OUT 55
RF21 R3G11 20 KOHM 1% EMPTY 402

FB2 10
VREG_VMEM_FB_MID OUT 55
RF22 R3G12 10 KOHM 1% EMPTY 402

VREG_VMEM_COMP 11 COMP2
CC21 C3G6 4700 PF 10% 50 V X7R 402
CC22 C3G7 22 PF 5% 50 V NPO 402
VREG_VMEM_COMP_C
RC2 R3V4 43.2 KOHM 1% CH 402

VREG_VMEM_SS 13 SS2
CSS1 C3G8 0.047 UF 10% 10 V X7R 402

X817911-002 LCC32

[PAGE_TITLE=[VREGS, VMEM]

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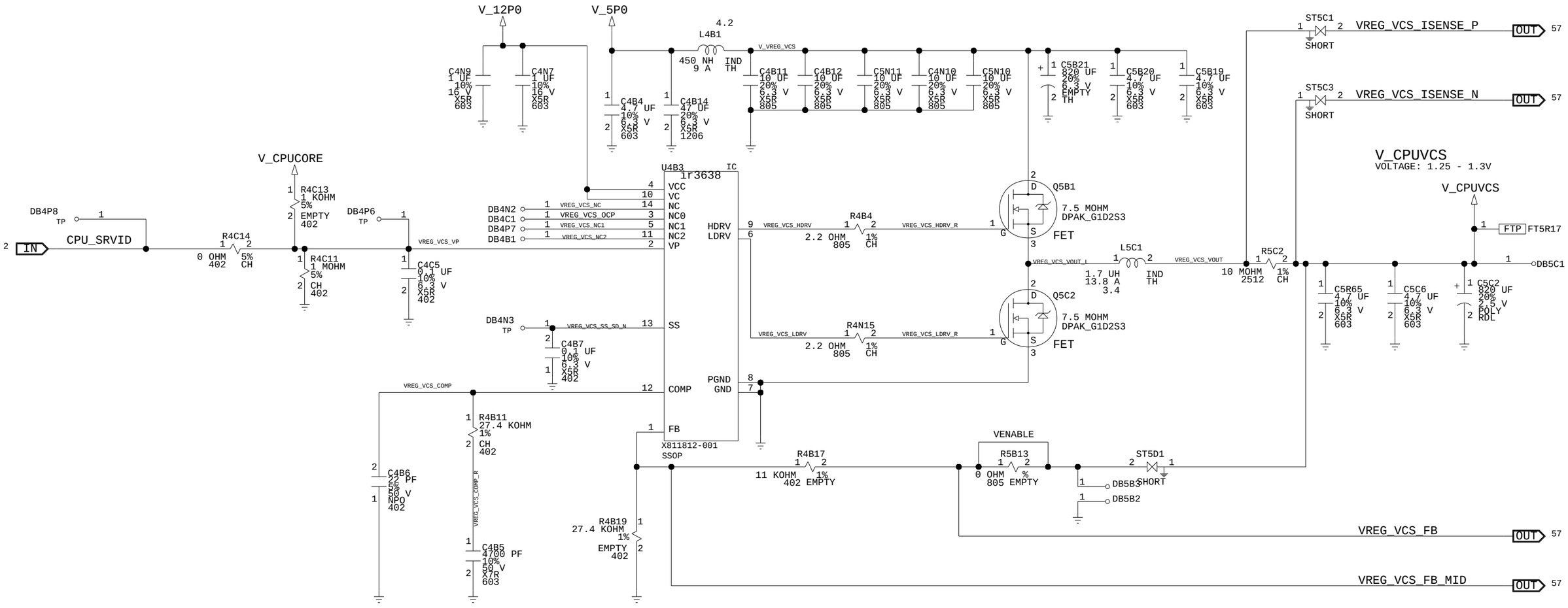
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	50/87	E	1.01

VREGS, VCS



GAIN=0.4 WITH R4B17 = 11K, R4B19 = 27.4K
OUTPUT = CPU_SRVID(1+GAIN)

[PAGE_TITLE=VREGS, VCS]

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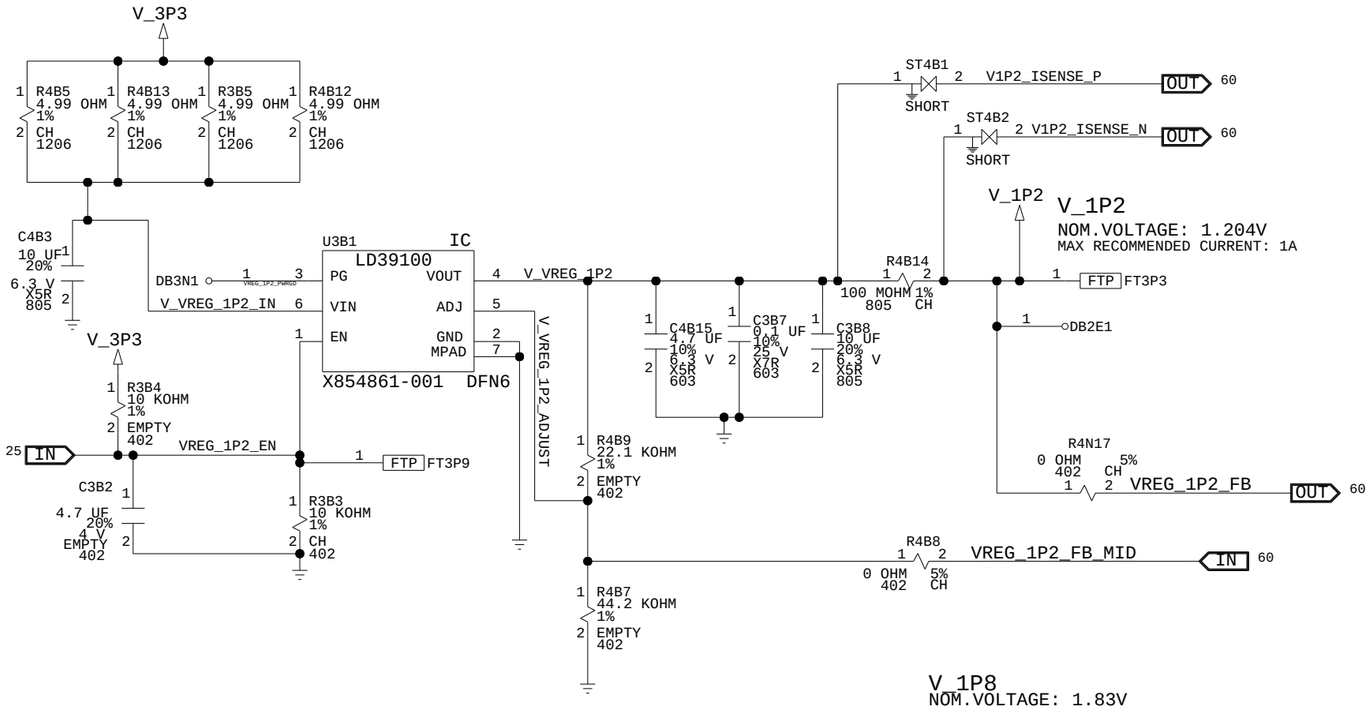
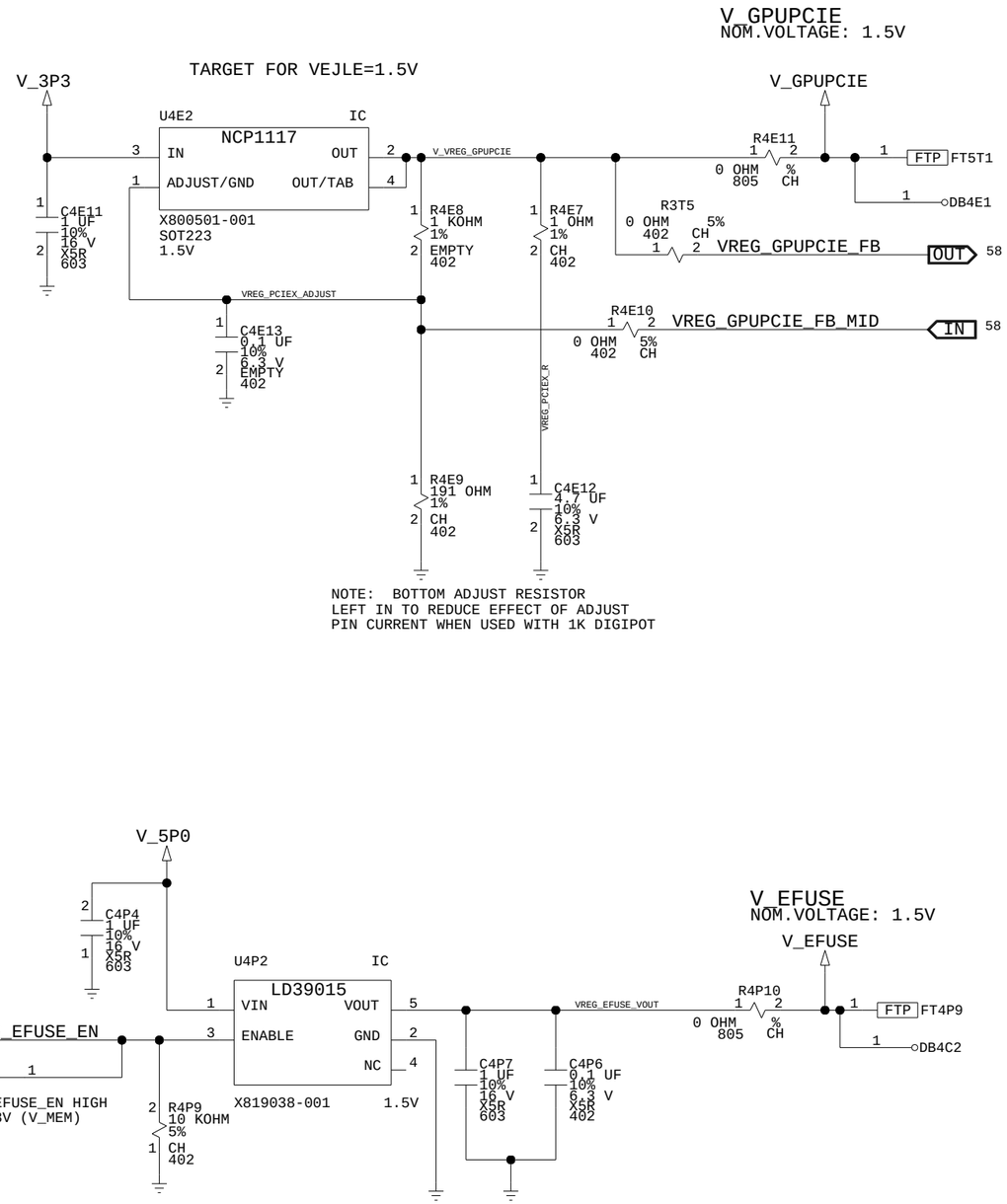
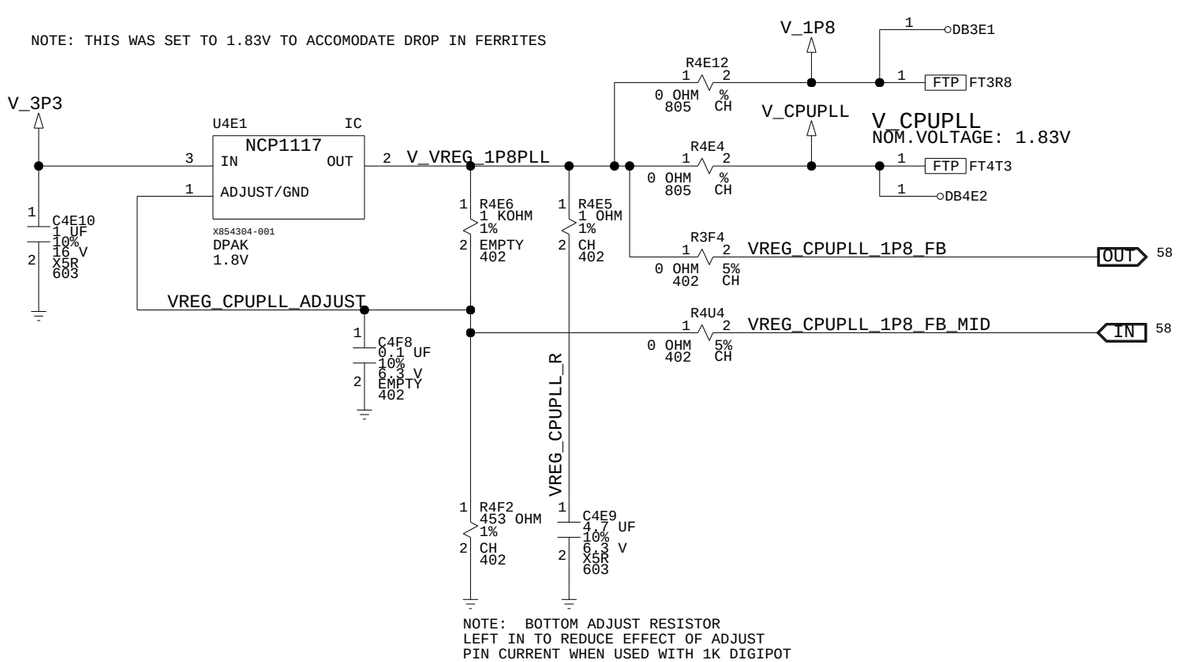
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	51/87	E	1.01

VREGS, 1P2+1P8+GPUPCIE+CPUPLL+EFUSE







[PAGE_TITLE=VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE]

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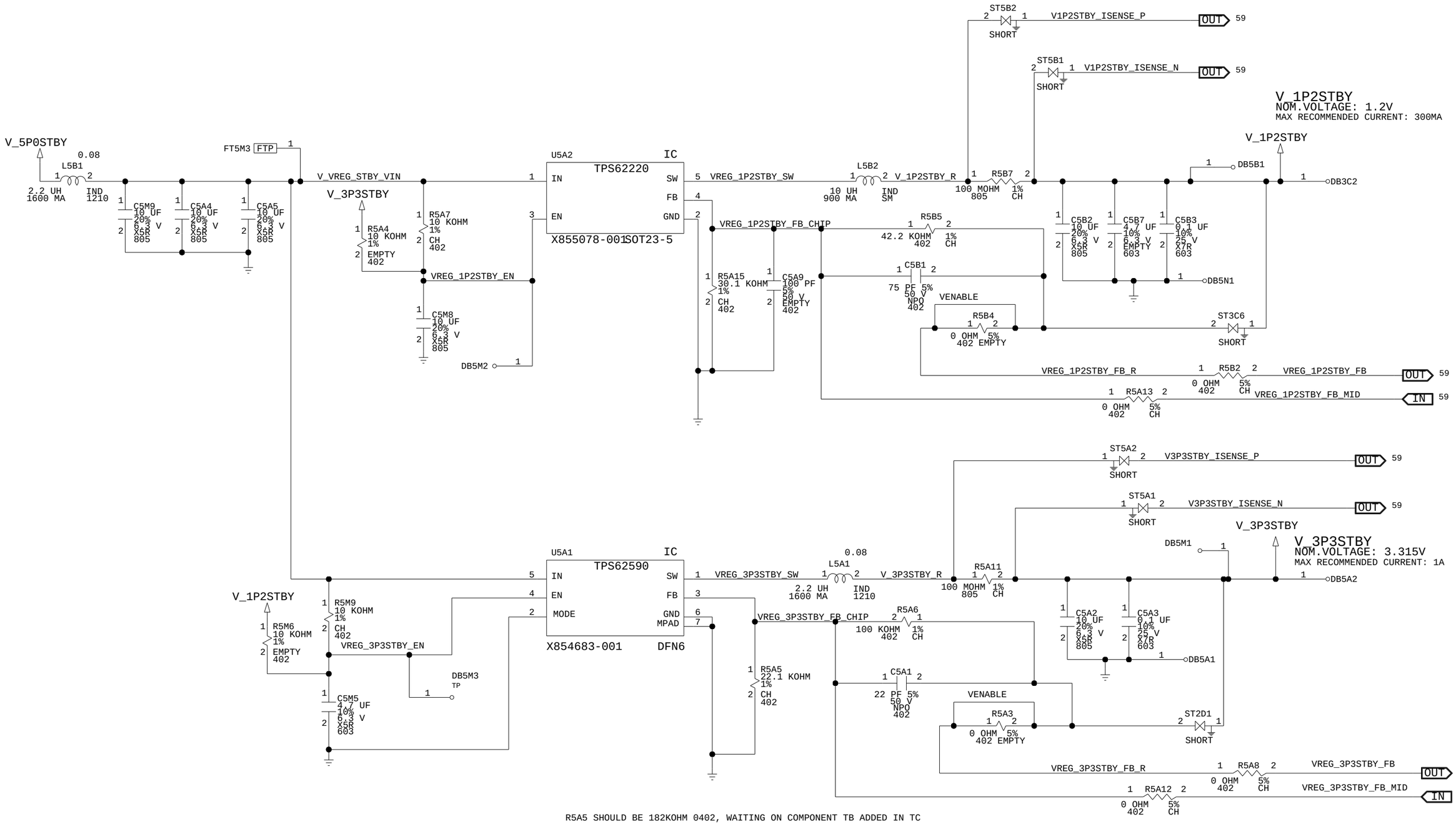
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	52/87	E	1.01

VREGS,STANDBY SWITCHERS



R5A5 SHOULD BE 182KOHM 0402, WAITING ON COMPONENT TB ADDED IN TC

[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

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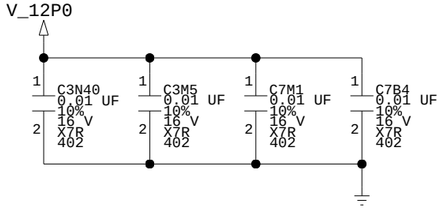
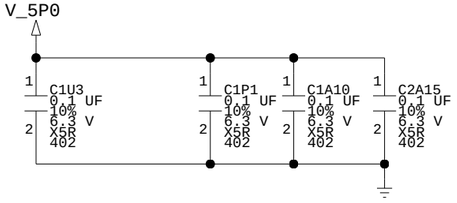
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	53/87	E	1.01

BOARD LEVEL DECOUPLING

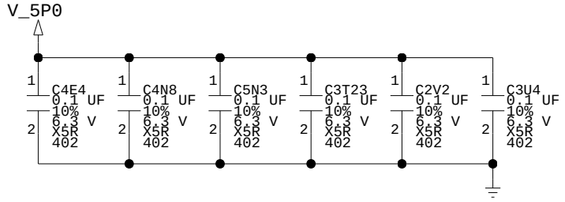
V_12P0



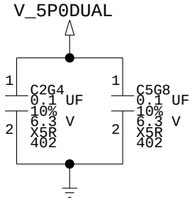
V_5P0



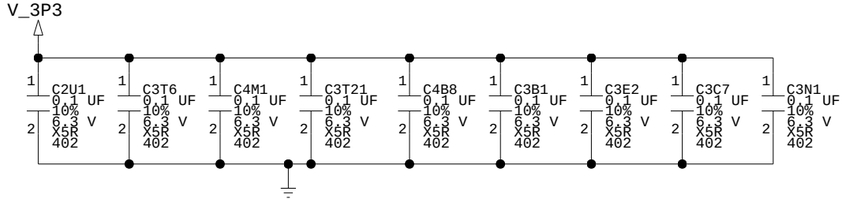
V_5P0



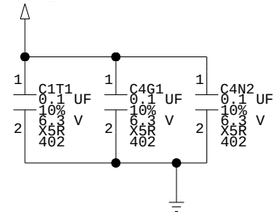
V_5P0DUAL



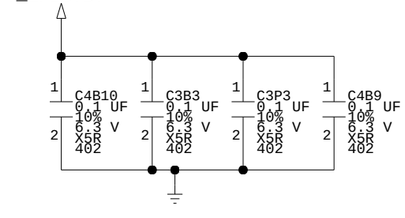
V_3P3



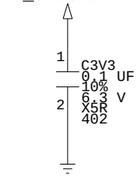
V_3P3STBY



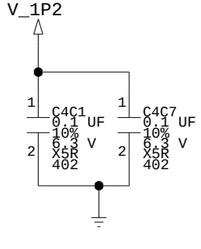
V_1P2STBY



V_5P0STBY



V_1P2



[PAGE_TITLE=BOARD, DECOUPLE]

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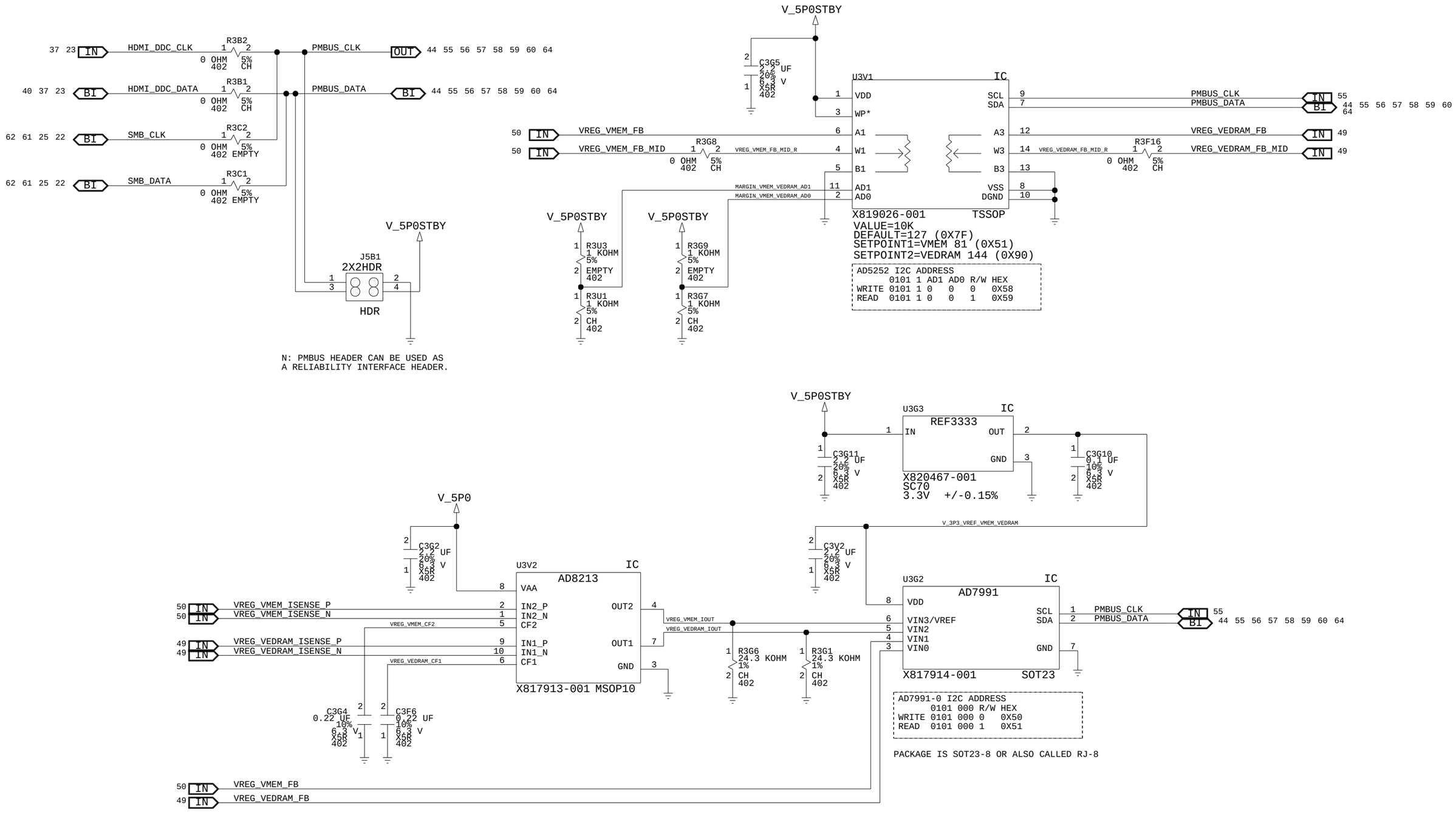
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	54/87	E	1.01

MARGIN, VMEM + VEDRAM



[PAGE_TITLE=MARGIN, VMEM + VEDRAM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	55/87	E	1.01

MARGIN, V3P3 + V5P0

47 IN VREG_V5P0_FB
R2U1 35.7 KOHM 1% 2 CH 402
V_P Q2F3 ADR5043 NC3 X819033-001 3.0V 0.1% V_N IC
V_5P0STBY
C2F4 2.2 UF 20% 6.3 V X5R 402
U1U1 IC
VDD WP* A1 W1 B1 AD1 AD0
SCL SDA A3 W3 B3 VSS DGND
PMBUS_CLK PMBUS_DATA
IN 55 B1 44 55 56 57 58 59 60 64
VREG_V5P0_FB_A1
VREG_V5P0_FB_MID_R
VREG_V3P3_FB_A3
VREG_V3P3_FB_MID_R
47 IN VREG_V5P0_FB_MID
R2T5 0 OHM 5% 402 CH
MARGIN_V3P3_V5P0_AD1
MARGIN_V3P3_V5P0_AD0
X819026-001 TSSOP
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=V5P0 69 (0X45)
SETPOINT2=V3P3 123 (0X7B)

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W HEX
WRITE 0101 1 0 1 0 0X5A
READ 0101 1 0 1 1 0X5B

V_5P0STBY
R1U4 1 KOHM 5% EMPTY 402
R1U3 1 KOHM 5% CH 402
V_5P0STBY
R2F3 1 KOHM 5% CH 402
R2F2 1 KOHM 5% EMPTY 402

VREG_V3P3_FB
IN 48
R1U5 22.1 KOHM 1% 2 CH 402
V_P Q1F1 NC3 X819034-001 2.048V 0.1% V_N IC ADR5040A
R1T19 0 OHM 5% 402 CH
VREG_V3P3_FB_MID
IN 48

V_5P0DUAL
U1F3 IC REF3333
IN OUT GND
C1F10 2.2 UF 20% 6.3 V X5R 402
C1F11 0.1 UF 10% 6.3 V X5R 402
X820467-001 SC70 3.3V +/-0.15%
V_3P3_VREF_V5P0_V3P3

V_5P0
C1U2 2.2 UF 20% 6.3 V X5R 402
U2U1 IC AD8213
VAA IN2_P IN2_N CF2 IN1_P IN1_N CF1 OUT2 OUT1 GND
47 IN VREG_V5P0_ISENSE_P
47 IN VREG_V5P0_ISENSE_N
48 IN VREG_V3P3_ISENSE_P
48 IN VREG_V3P3_ISENSE_N
VREG_V5P0_CF2
VREG_V3P3_CF1
C2F6 0.22 UF 10% 6.3 V X5R 402
C1F2 0.22 UF 10% 6.3 V X5R 402
X817913-001 MSOP10
VREG_V5P0_IOUT
VREG_V3P3_IOUT
R2F5 24.3 KOHM 1% 2 CH 402
R2F8 24.3 KOHM 1% 2 CH 402
V_5P0
R2F4 150 OHM 1% 402 CH
VREG_V5P0_FB_R
V_3P3
R1F4 150 OHM 1% 402 CH
VREG_V3P3_FB_R
R1F6 221 OHM 1% 2 CH 402
R1F5 221 OHM 1% 2 CH 402

C2F2 2.2 UF 20% 6.3 V X5R 402
U1F2 IC AD7991
VDD VIN3/VREF VIN2 VIN1 VIN0 SCL SDA GND
PMBUS_CLK
PMBUS_DATA
IN 55 B1 44 55 56 57 58 59 60 64
X818998-001 SOT23

AD7991-1 I2C ADDRESS
0101 001 R/W HEX
WRITE 0101 001 0 0X52
READ 0101 001 1 0X53

PACKAGE IS SOT23-8 OR ALSO CALLED RJ-8

[PAGE_TITLE=MARGIN, V3P3 + VP50]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	56/87	E	1.01

MARGIN, VREFS + VCS

V_5P0STBY
U5B6 IC
REF3333
X820467-001
SC70
3.3V +/-0.15%
C5N8 2.2 UF 20% 6.3 V X5R 402
C5N7 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_VCS
C5N1 2.2 UF 20% 6.3 V X5R 402

U4B2 IC
AD7992
X814249-001 MSOP10
VDD, SCL, SDA, VIN2/REFIN, VIN1, AS, CONVST_N*, ALERT/BUSY, AGND2, AGND1
PMBUS_CLK
PMBUS_DATA
57 IN MEM_VREFS
MARGIN_VIN1
R5B14 1 KOHM 5% CH 402
R5B16 1 KOHM 5% EMPTY 402
MARGIN_VREFS_AS
MARGIN_VREFS_CONVST
R5B15 1 KOHM 5% CH 402
R4N10 1 KOHM 5% CH 402

AD7992-1 I2C ADDRESS
AS=GND 0100011 R/W
WRITE 0100011 0 0X46
READ 0100011 1 0X47
AS=VDD 0100100 R/W HEX

57 51 IN VREG_VCS_FB

V_5P0
C5B15 2.2 UF 20% 6.3 V X5R 402
U5B2 IC
AD8213
X817913-001 MSOP10
VAA, IN2_P, IN2_N, CF2, IN1_P, IN1_N, CF1, OUT2, OUT1, GND
VREG_VCS_CF2
VREG_VCS_CF1
VREG_VCS_IN
VREG_VCS_IOUT2
VREG_VCS_IOUT
51 IN VREG_VCS_ISENSE_P
51 IN VREG_VCS_ISENSE_N
C5B4 0.22 UF 10% 6.3 V X5R 402
C5B8 0.22 UF 10% 6.3 V X5R 402
R5B10 1 KOHM 5% CH 402
R5B12 24.3 KOHM 1% CH 402
R5N2 24.3 KOHM 1% CH 402
C5N2 2.2 UF 20% 6.3 V X5R 402

U5B1 IC
AD7992
X814249-001 MSOP10
VDD, SCL, SDA, VIN2/REFIN, VIN1, AS, CONVST_N*, ALERT/BUSY, AGND2, AGND1
PMBUS_CLK
PMBUS_DATA
R5B6 1 KOHM 5% CH 402
MARGIN_VCS_AS
MARGIN_VCS_CONVST
R5B11 1 KOHM 5% EMPTY 402
R5N1 1 KOHM 5% CH 402

AD7992-1 I2C ADDRESS
AS=VDD 0100100 R/W HEX
WRITE 0100100 0 0X48
READ 0100100 1 0X49
AS=GND 0100011 R/W

V_5P0STBY
V_MEM
C4N1 2.2 UF 20% 6.3 V X5R 402
U4B1 IC
VDD, WP*, A1, W1, B1, AD1, AD0, SCL, SDA, A3, W3, B3, VSS, DGND
PMBUS_CLK
PMBUS_DATA
VREG_VCS_FB
VREG_VCS_FB_MID
57 OUT MEM_VREFS
R4N5 0 OHM 5% CH 402 MEM_VREFS_R
R4B18 0 OHM 5% CH 402 VREG_VCS_FB_MID_R
MARGIN_VREFS_AD1
MARGIN_VREFS_AD0
X819026-001 TSSOP
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=VREFS 63 (0X3F)
SETPOINT2=VCS 140 (0X8C)

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W
WRITE 0101 1 1 1 0 0X5E
READ 0101 1 1 1 1 0X5F

V_5P0STBY R4N2 1 KOHM 5% CH 402
V_5P0STBY R4N7 1 KOHM 5% CH 402
V_MEM R4N4 100 OHM 5% CH 402
R4N3 1 KOHM 5% EMPTY 402
R4N6 1 KOHM 5% EMPTY 402
MARGIN_VMEM_VREFS_BOT

Q4B1 ADR510 X821158-001 1.0V 0.35% IC
V_P, NC, V_N

[PAGE_TITLE=MARGIN, VREFS + VCS]

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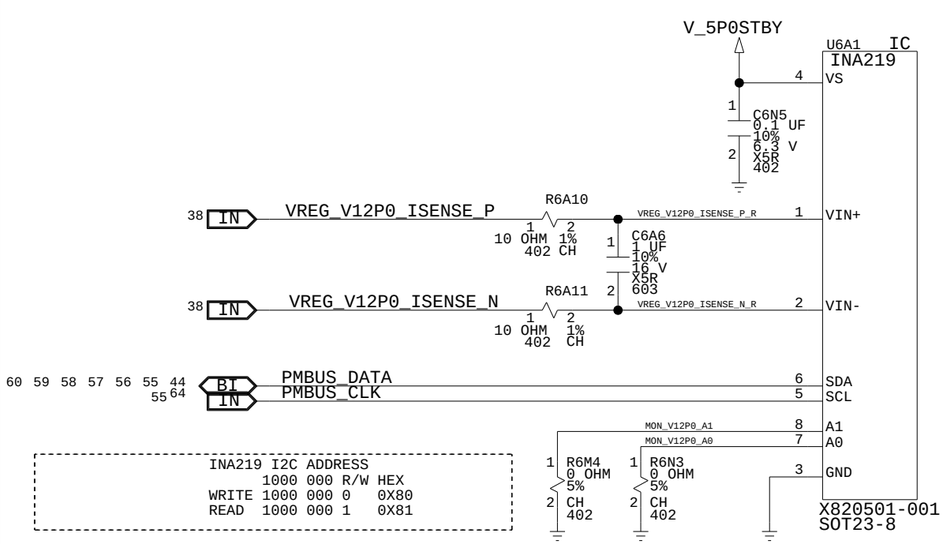
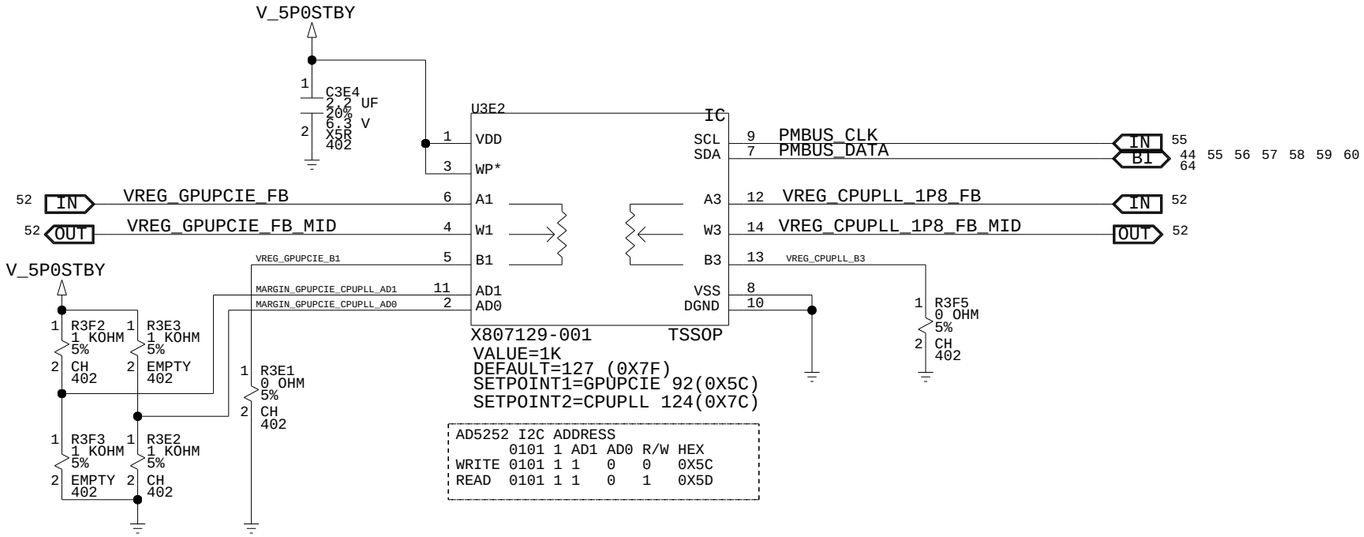
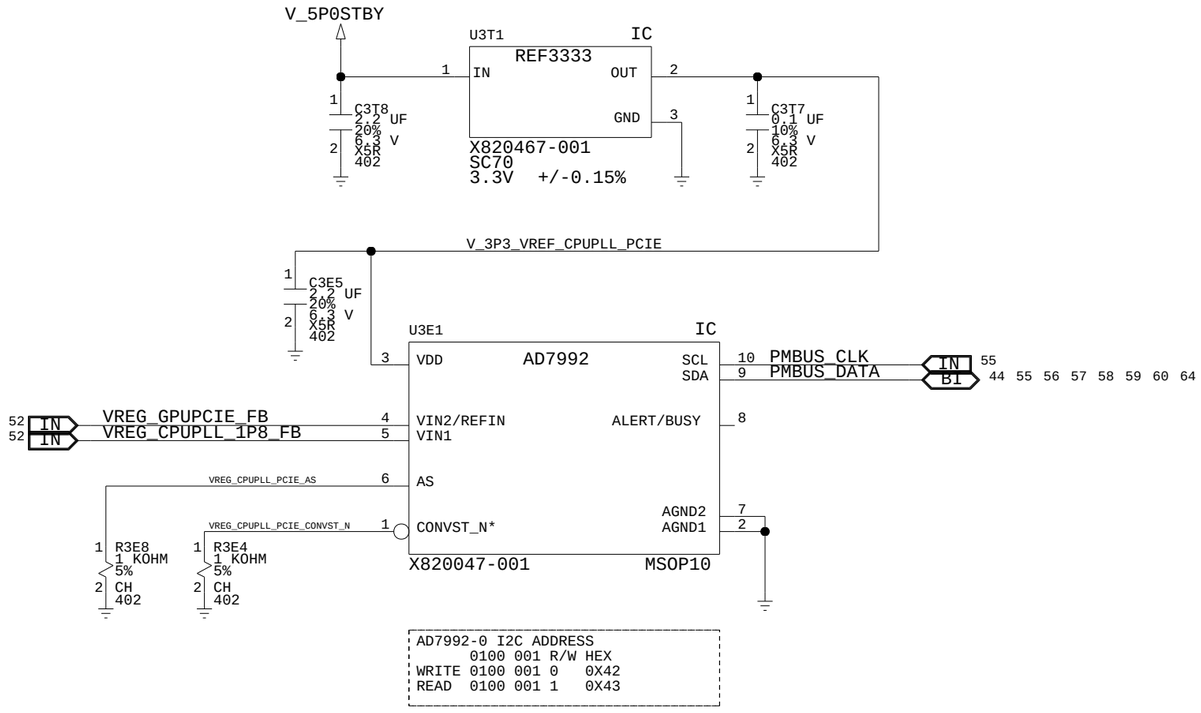
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	57/87	E	1.01

MARGIN, VGPUPCIE,1P8, VCPUPLL, V12P0, TEMP







[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	58/87	E	1.01

MARGIN, STANDBY

INA219 I2C ADDRESS
1001 100 R/W HEX
WRITE 1001 100 0 0X98
READ 1001 100 1 0X99

V_5P0STBY
U5N3 IC INA219
C6N6 0.1 UF 10% 6.3 V X5R 402
R6N4 10 OHM 1% 402 CH
C6N4 1 UF 10% 16 V X5R 603
R6N5 10 OHM 1% 402 CH
R5N5 3.32 KOHM 1% 402 CH
R5N3 0 OHM 5% 402 CH
38 IN V5P0STBY_ISENSE_P
38 IN V5P0STBY_ISENSE_N
60 59 58 57 56 55 44 64 BI PMBUS_DATA
55 IN PMBUS_CLK
MON_V5P0STBY_A1
MON_V5P0STBY_A0
VIN+ VIN- SDA SCL A1 A0 GND
X820501-001 SOT23-8

V_5P0STBY
U5A3 IC MCP4661
R5A14 1 KOHM 5% 402 CH
R5B1 20 KOHM 1% 402 CH
R5M14 1 KOHM 5% 402 CH
R5B3 1 KOHM 5% 402 CH
C5N4 0.1 UF 10% 6.3 V X5R 402
R5M15 178 KOHM 1% 402 CH
53 IN VREG_1P2STBY_FB
53 OUT VREG_1P2STBY_FB_MID
VREG_1P2STBY_FB_D
VREG_3P3STBY_FB
VREG_3P3STBY_FB_D
VREG_3P3STBY_FB_MID
60 59 58 57 56 55 44 64 BI PMBUS_DATA
55 IN PMBUS_CLK
MARGIN_STBY_A2
MARGIN_STBY_A1
MARGIN_STBY_A0
P1B P1W P1A P0B P0W P0A SCL SDA A2 A1 HVC/A0 VDD WP_N VSS2 VSS MPAD NC
X854038-001

MCP4661 I2C ADDRESS
0101 AD2 AD1 AD0 R/W HEX
WRITE 0101 0 1 0 0 0X54
READ 0101 0 1 0 1 0X55

BUGBUG: NEED TO DECIDE R VALUE
BUGBUG: FOR NOMINAL VOLTAGE OF 1.2V

INA219 I2C ADDRESS
1001 000 R/W HEX
WRITE 1001 001 0 0X92
READ 1001 001 1 0X93

V_5P0STBY
U5M1 IC INA219
C5M6 0.1 UF 10% 6.3 V X5R 402
R5M11 10 OHM 1% 402 CH
C5M7 1 UF 10% 16 V X5R 603
R5M10 10 OHM 1% 402 CH
R5M13 3.32 KOHM 1% 402 CH
R5M12 0 OHM 5% 402 CH
53 IN V3P3STBY_ISENSE_P
53 IN V3P3STBY_ISENSE_N
64 60 59 58 57 56 55 44 BI PMBUS_DATA
55 IN PMBUS_CLK
MON_V3P3STBY_A1
MON_V3P3STBY_A0
VIN+ VIN- SDA SCL A1 A0 GND
X820501-001 SOT23-8

INA219 I2C ADDRESS
1000 011 R/W HEX
WRITE 1000 011 0 0X86
READ 1000 011 1 0X87

V_5P0STBY
U5N2 IC INA219
C5N9 0.1 UF 10% 6.3 V X5R 402
R5M16 10 OHM 1% 402 CH
C5M10 1 UF 10% 16 V X5R 603
R5N4 10 OHM 1% 402 CH
R4N9 0 OHM 5% 402 CH
R4N11 3.32 KOHM 1% 402 CH
53 IN V1P2STBY_ISENSE_P
53 IN V1P2STBY_ISENSE_N
64 60 59 58 57 56 55 44 BI PMBUS_DATA
55 IN PMBUS_CLK
MON_V1P2STBY_A1
MON_V1P2STBY_A0
VIN+ VIN- SDA SCL A1 A0 GND
X820501-001 SOT23-8

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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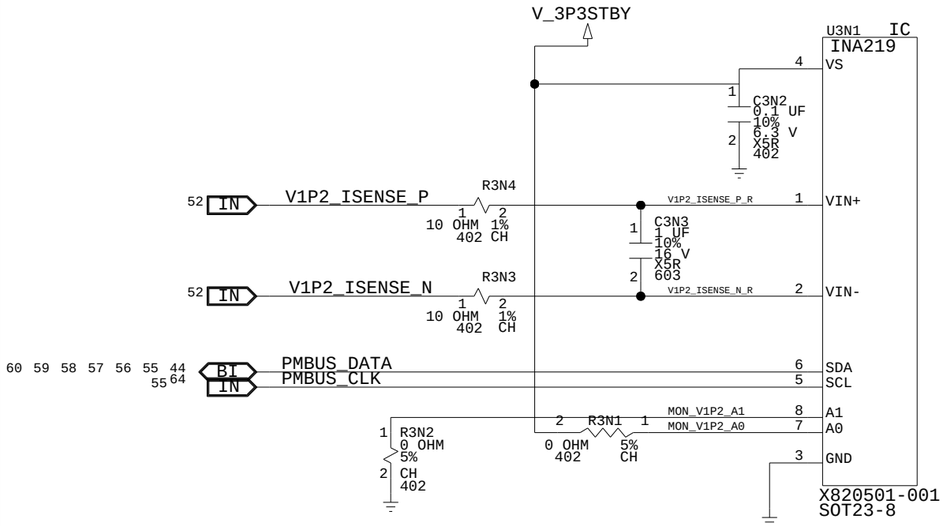
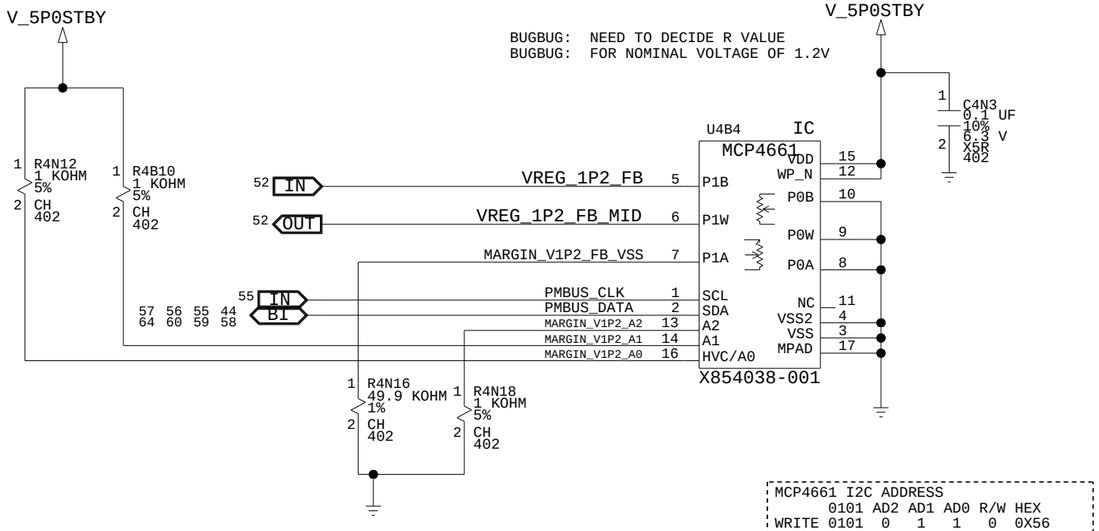
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	59/87	E	1.01

MARGIN, V1P2



INA219 I2C ADDRESS

	1000	100	R/W	HEX
WRITE	1000	001	0	0X82
READ	1000	001	1	0X83



MCP4661 I2C ADDRESS

	0101	AD2	AD1	AD0	R/W	HEX
WRITE	0101	0	1	1	0	0X56
READ	0101	0	1	1	1	0X57

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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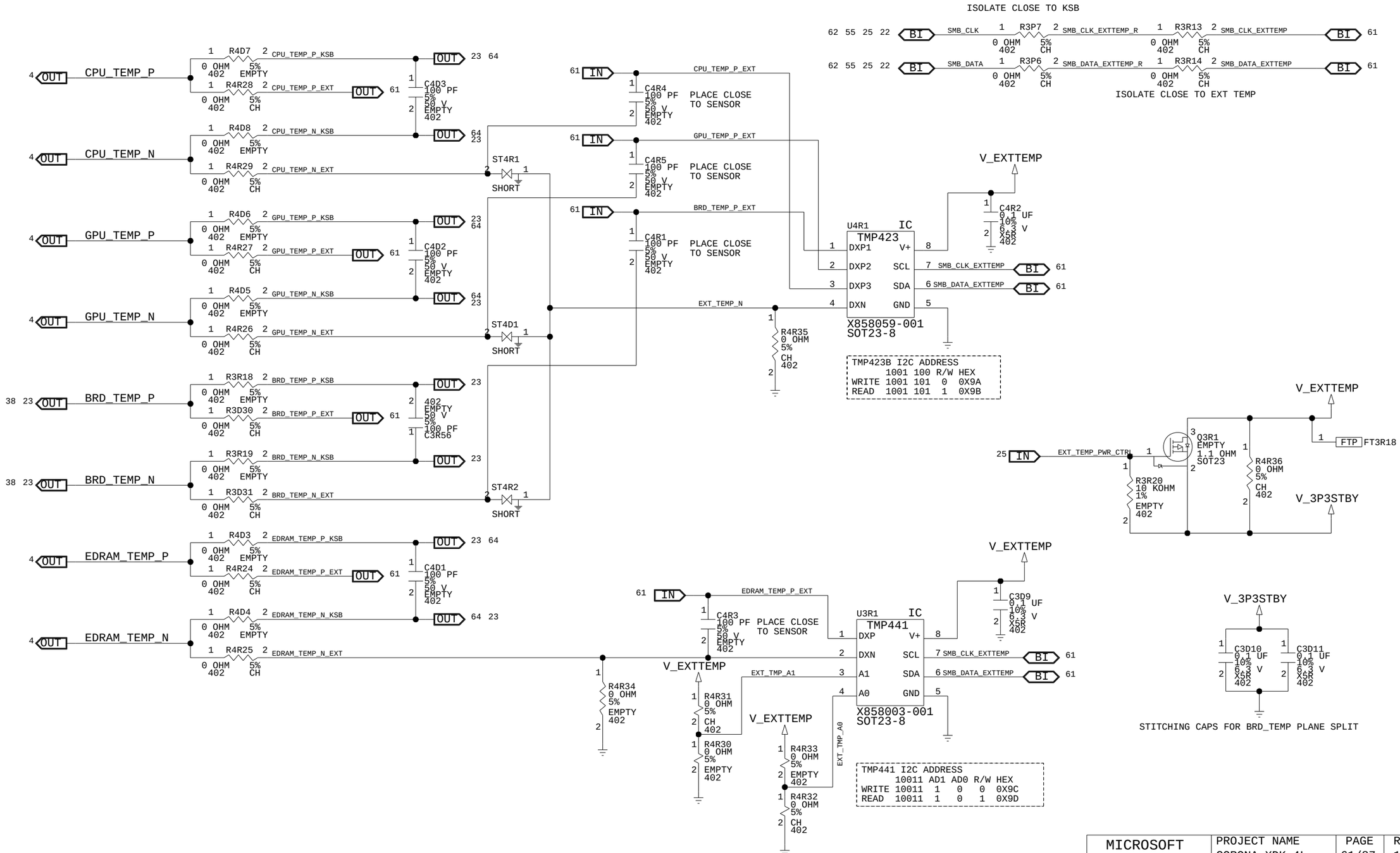
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	60/87	E	1.01

EXTERNAL TEMP SENSORS



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	CORONA_XDK_4L	61/87	1.01

XDK, DEBUG CONNECTORS

KSB DEBUG BUS

J2C2 EMPTY

2X13SOFTTOUCH

24	IN	FAN_TACH_SMM_R	A1	A_D1	B_D0	B1	WSS_CNTL1	IN	24
24	IN	WSS_CNTL0	A2	A_D3	B_D2	B2	SCART_RGB	IN	24
			A3	A_GND1	B_GND0	B3			
24	IN	SB_GPIO<4>	A4	A_D5	B_D4	B4	SB_GPIO<1>	IN	24
			A5	A_D7	B_D6	B5	SB_GPIO<0>	IN	24
			A6	A_GND3	B_GND2	B6			
24	IN	SB_GPIO<2>	A7	A_D9	B_D8	B7	SB_GPIO<3>	IN	24
24	IN	AUD_SPI_CLK_R	A8	A_D11	B_D10	B8	AUD_SPI_MOSI_R	IN	24
			A9	A_GND5	B_GND4	B9			
24	IN	AUD_RDY_BSBY_R	A10	A_D13	B_D12	B10	SB_GPIO<5>	IN	24
24	IN	AUD_SSB_R	A11	A_D15	B_D14	B11	AUD_SPI_MISO_R	IN	24
			A12	A_GND7	B_GND6	B12			
			A13	A_NC	B_CLK	B13			
			27	MH1	MH3	29			
			28	MH2	MH4	30			

X854421-001

PHY MDIO INTERFACE

NET NAME	MDIO SIGNAL
SB_GPIO<1>	PCIE MDC
SB_GPIO<0>	PCIE MDIO
SB_GPIO<2>	FPHY MDIO
SB_GPIO<3>	FPHY MDC
SB_GPIO<5>	SATA0 MDC
SB_GPIO<4>	SATA0 MDIO
AUD_SPI_MOSI_R	SATA1 MDC
AUD_SPI_CLK_R	SATA1 MDIO
WSS_CNTL0	USGBRPA MDC
WSS_CNTL1	USGBRPA MDIO
AUD_RDY_BSBY_R	USGBRPB MDC
FAN_TACH	USGBRPB MDIO

J2C1

2X5HDR10

26	OUT	SPI_SS_N	2	1	SPI_MOSI	OUT	26
26	IN	SPI_MISO	4	3	SPI_CLK	OUT	26
			6	5			
			8	7			
				9			

HDR

V_5P0STBY

C2C3 0.1 UF 10% 6.3 V X5R 402

PCIEX DEBUG CONNECTOR
N: DEBUG BOARDS ONLY

V_3P3

C4A12 0.1 UF 10% 6.3 V X5R 402

J2C3

2X7HDR14

24	IN	KER_DBG_TXD	2	1			
25	IN	SMC_DBG_TXD	4	3			
25	OUT	SMC_DBG_EN	6	5	SMC_RST_XDK_N	1 R2C10 2	SMC_RST_N IN 22
			8	7			
		SMB_CLK_R	10	9			
			12	11			
				13			

HDR

100 OHM 5% 402 CH

KER_DBG_RXD OUT 24

SMC_DBG_RXD_R OUT 62

61 55 25 22 BI SMB_CLK 1 R2C6 2 100 OHM 5% 402 CH

V_3P3STBY

C2C4 0.1 UF 10% 6.3 V X5R 402

C2B4 1 UF 10% 16 V X5R 603

V_5P0STBY

C2C5 0.1 UF 10% 6.3 V X5R 402

C2C6 1 UF 10% 16 V X5R 603

SMB_DATA_R 1 R2C7 2 SMB_DATA BI 22 25 55 61

100 OHM 5% 402 CH

EXT_PWR_ON_DBG 1 R2C4 2 EXT_PWR_ON_N OUT 37 63 25 64

1 KOHM 5% 402 CH

I258

SM

J3E1 EMPTY

PCIEX MIDBUS

24	IN	PEX_SB_GPU_L0_DP	2	1	PEX_GPU_SB_L0_DP	IN	4		
24	IN	PEX_SB_GPU_L0_DN	4	3	PEX_GPU_SB_L0_DN	IN	4		
			6	5					
			8	7	PEX_GPU_SB_L1_DP	IN	4		
24	IN	PEX_SB_GPU_L1_DP	10	9	PEX_GPU_SB_L1_DN	IN	4		
24	IN	PEX_SB_GPU_L1_DN	12	11					
			14	13					
			16	15					
			18	17					
			20	19					
			22	21					
			24	23					

X801071-001

N: FOOTPRINT PADS 13-24 REMOVED.
N: REMOVED PADS FREE UP NEEDED
BOARD SPACE FOR ROUTING.

J4D2

1X3HDR

22 IN GPU_CLK_DN 1

22 IN GPU_CLK_DP 2

3

EMPTY

62 IN SMC_DBG_RXD_R 1 R2C2 2 SMC_DBG_RXD OUT 25

100 OHM 5% 402 CH

C2C1 0.01 UF 10% 16 V X7R 402

[PAGE_TITLE=XDK. DEBUG CONN]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	62/87	E	1.01

XDK DEBUG

GCPU JTAG HEADER

J4C1
2X4HDR

CPU_TDI
CPU_TDO
CPU_TCLK
CPU_TRST_N_R
CPU_TMS
GPU_TRST_N
GPU_TRST_ED_N

HDR

GCPU EEPROM HEADER

J4C3
2X3HDR

GPU_SROM_SCLK_R
GPU_SROM_SO_R
GPU_SROM_CS_N_R
GPU_SROM_SI
GPU_SROM_WP_N

HDR

SB JTAG HEADER

J3E2
2X3HDR

SB_TDI
SB_TDO
SB_TCLK
SB_TMS
SB_TRST

HDR

FTPS LOCKED FOR FUTURE REVISION

FT5T2 FTP 1
LOCATE AT: 4935, 2845

FT4P11 FTP 1
LOCATE AT: 4495, 4560

V_5P0

DB2E4 1
DB1D2 1

V_3P3

DB2C5 1

GND VIAS

DB2B1 1
DB2B2 1
DB1C1 1
DB2C3 1
DB4B2 1
DB2B3 1
DB2C4 1
DB1B1 1
DB1D1 1
DB2G5 1
DB3E2 1
DB4C3 1
DB3C4 1
DB4D1 1

V_5P0DUAL

U2V1 IC
SN74LVC1G14
VCC
IN
GND
OUT
N/C
X801189-001

25 IN DBG_LED0
DBG_LED0_LED_R
R2V1
249 OHM 1% 402 CH
DBG_LED0_LED
D2G1
YELLOW LED SM

U1D1
2X8RCPT

FLSH_CE_N
FLSH_DATA<7>
FLSH_DATA<6>
FLSH_DATA<4>
FLSH_DATA<2>
FLSH_DATA<0>
MMC_RST_N
FLSH_WP_N
FLSH_DATA<5>
FLSH_DATA<3>
FLSH_DATA<1>

RCPT

V_3P3STBY

C1R2 4.7 UF 10% 6.3 V X5R 603
C1R1 0.1 UF 10% 6.3 V X5R 402
C1R3 0.1 UF 10% 6.3 V X5R 402

V_3P3

C2F7 0.1 UF 10% 6.3 V EMPTY 402
C2F5 4.7 UF 10% 6.3 V X5R 805

V_5P0

D4P1 GREEN SM 2 LED

V_MEM

C4C4 0.1 UF 10% 6.3 V X5R 402
R4P8 10 KOHM 5% EMPTY 402

V_3P3STBY

R3P1 10 KOHM 5% CH 402

25 IN CPU_PWRGD
R2F6 5% 1 KOHM CH 402
CPU_PWRGD_R
J2F1
1X3HDR
HDR

R4P1 825 OHM 1% 402 CH
CPU_CHECKSTOP_N_LED
CPU_CHECKSTOP_N_LED_C

R4P2 1 KOHM 5% 402 CH
CPU_CHECKSTOP_N_LED_B
Q4C2 XSTR

R4C4 1 KOHM 5% 402 CH
SMC_CPU_CHKSTOP_DETECT_B
Q4C1 XSTR

SMC_CPU_CHKSTOP_DETECT BI 25

2 IN CPU_RST_V1P1_N
R4P3 1 KOHM 5% 402 EMPTY
CPU_RST_N_2_R

J4C2
2X5HDR

CPU_TMS
CPU_TRST_N
CPU_TDO
CPU_TDI
CPU_CHECKSTOP_N_R

HDR

C4C3 0.1 UF 10% 6.3 V X5R 402

R4C7 0 OHM 5% 402 CH
CPU_CHECKSTOP_N
IN 2

CPU_TCLK OUT 5 63
EXT_PWR_ON_N OUT 37 62 25 64

PWR LEDS

V_12P0 V_5P0 V_5P0STBY V_3P3 V_3P3STBY

R7A3 3.32 KOHM 1% CH 402
R2G8 1 KOHM 1% CH 402
R6A7 1 KOHM 1% CH 402
R4A8 330 OHM 1% CH 402
R4B6 330 OHM 1% CH 402

V_12P0_LED_R
V_5P0_LED_R
V_5P0STBY_LED_R
V_3P3_LED_R
V_3P3STBY_LED_R

LED SM GREEN
D7A1 D2G2 D6A1 D5A1 D4B1

[PAGE_TITLE=XDK, DEBUG TITAN]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	65/87	E	1.01

DEBUG BOARD, SPYDER CONN

ALL STP POINTS SHALL BE ADDED TO TOP SIDE IN LAYOUT

V_MEM
- 1 — STP7E1
- 1 — STP7E2

V_CPUVCS
- 1 — STP5D1
- 1 — STP5D2

V_CPUEDRAM
- 1 — STP4E2
- 1 — STP4E1

V_CPUCORE
- 1 — STP6C1
- 1 — STP6C2

V_CPUPLL
- 1 — STP4E3

61 23 IN CPU_TEMP_P_KSB 1 — STP4D4

STP4D5 1 CPU_TEMP_N_KSB OUT 61 23

61 23 IN EDRAM_TEMP_P_KSB 1 — STP3D1

STP4D1 1 EDRAM_TEMP_N_KSB OUT 61 23

61 23 IN GPU_TEMP_P_KSB 1 — STP4D3

STP4D2 1 GPU_TEMP_N_KSB OUT 61 23

43 IN VREG_CPU_VID<1..6>
- 1 — STP7C7
- 2 — STP7C6
- 3 — STP7C5
- 4 — STP7C4
- 5 — STP7C3
- 6 — STP7C2

44 IN VREG_CPU_CSSUM 1 — STP7B1
44 IN VREG_CPU_CSCOMP 1 — STP7C1
44 IN VREG_CPU_CSREF 1 — STP7N1

63 62 37 IN EXT_PWR_ON_N 1 — STP3C1

60 59 58 57 56 55 44 BI PMBUS_DATA 1 — STP5B1
55 IN PMBUS_CLK 1 — STP5B2

GND FTS FOR TEST FIXTURES

FT3M12 FTP		FT1R2 FTP	
FT1P3 FTP		FT6N1 FTP	
FT1T11 FTP		FT7M1 FTP	
FT3N1 FTP		FT2T6 FTP	
FT2N2 FTP		FT4V1 FTP	
FT3N4 FTP		FT2T7 FTP	
FT3T9 FTP		FT3N2 FTP	
FT2V4 FTP		FT1P2 FTP	
FT4R1 FTP		FT2N1 FTP	
FT7N2 FTP		FT6V1 FTP	

[PAGE_TITLE=DEBUG BOARD, SPYDER CONN]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	66/87	E	1.01

LABELS AND MOUNTING

INTELLIGENT SERIAL NUMBER TARGET.

LB2B1
LABEL
1
1375X250_TARGET
X801181-001

WEST PCB MOUNTING HOLES

EDGE
MTG1B1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG1G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG4G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EAST PCB MOUNTING HOLES

EDGE
MTG7G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

HEAT SINK MOUNTING HOLES

STD
MTG4F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG4D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

[PAGE_TITLE=LABELS AND MOUNTING]

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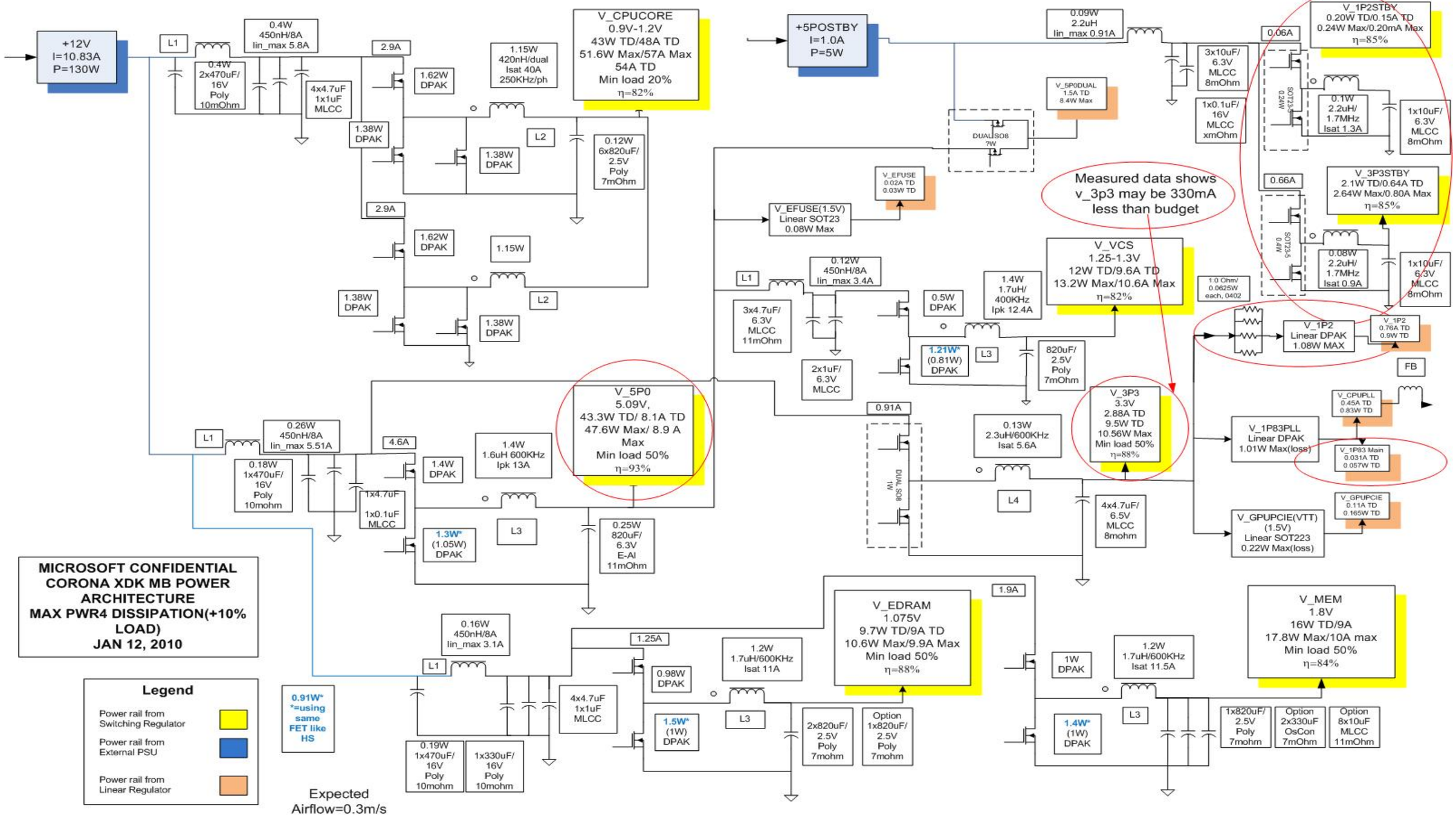
POWER ARCHITECTURE



<PAGE_TITLE=POWER ARCHITECTURE>

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TRINITY_FAB_A
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<PAGE_TITLE=SYSTEM BLOCK DIAGRAM>

RESET/ENABLE DIAGRAM

WAVE CONN
USB TRIPPLE CONN
RJ45 AUX CONN
HDMI CONN
AVIP CONN
TOSLINK CONN
POWER CONN
EXT_PWR_ON_N
AUD_RST_N
AUDIO DAC
FAN CONN
PSU_V12P0_EN
HDD SATA CONN
ODD SATA CONN
ODD PWR CONN
HDD PWR CONN
STANDBY SWITCHERS VR
CPU VR
VCS VR
DEBUG CONN
VREG_V1P2_EN
V1P2 VR
V5P0 DUAL VR
EXT_PWR_ON_N
SMC_DBG_EN
SMC_RST_N
VREG_CPU_EN
VREG_CPUCORE_PWRGD
CPU_RST_N
CPU_PWRGD
GPU_RST_N
GPU_RST_DONE
KSB
GCPU
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN
MEM A & B CLAM
FLASH
V5P0 V3P3 VR
VREG_V5P0_EN
VREG_V3P3_EN
VEFUSE VR
VREG_EFUSE_EN
VGPUPCIE VR
V1P8 VR
VREG_VEDRAM_EN
VREG_VMEM_EN
VEDRAM VMEM VR
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN
MEM C & D CLAM
TILT
PWR BUTTON
EJECT BUTTON
BORON FPM
IR
2 X GAME CONN

COMPONENT STUFFING TABLES

MARGIN REF DES TO STUFF

REFDES	DBG/XDK	RETAIL
C1F2	STUFF	NO-STUFF
C1F10	STUFF	NO-STUFF
C1F11	STUFF	NO-STUFF
C1G7	STUFF	NO-STUFF
C1G8	STUFF	NO-STUFF
C1G9	STUFF	NO-STUFF
C1G10	STUFF	NO-STUFF
C1G11	STUFF	NO-STUFF
C1G12	STUFF	NO-STUFF
C1G13	STUFF	NO-STUFF
C1U2	STUFF	NO-STUFF
C2F2	STUFF	NO-STUFF
C2F4	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C2E4	STUFF	NO-STUFF
C2E5	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C3G11	STUFF	NO-STUFF
C3G2	STUFF	NO-STUFF
C3G4	STUFF	NO-STUFF
C3U2	STUFF	NO-STUFF
C3U3	STUFF	NO-STUFF
C3V2	STUFF	NO-STUFF
C4B1	STUFF	NO-STUFF
C4N1	STUFF	NO-STUFF
C4N4	STUFF	NO-STUFF
C5B15	STUFF	NO-STUFF
C5B5	STUFF	NO-STUFF
C5B8	STUFF	NO-STUFF
C5N7	STUFF	NO-STUFF
C5N8	STUFF	NO-STUFF
C6A6	STUFF	NO-STUFF
C6M5	STUFF	NO-STUFF
J1G3	STUFF	NO-STUFF
Q1F1	STUFF	NO-STUFF
Q2F3	STUFF	NO-STUFF
Q4B1	STUFF	NO-STUFF
R1F4	STUFF	NO-STUFF
R1F5	STUFF	NO-STUFF
R1F6	STUFF	NO-STUFF
R1G1	STUFF	NO-STUFF
R1T19	STUFF	NO-STUFF
R1U3	STUFF	NO-STUFF
R1U4	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R1U5	STUFF	NO-STUFF
R2B1	STUFF	NO-STUFF
R2B3	STUFF	NO-STUFF
R2F2	STUFF	NO-STUFF
R2F3	STUFF	NO-STUFF
R2F4	STUFF	NO-STUFF
R2F5	STUFF	NO-STUFF
R2F8	STUFF	NO-STUFF
R2T5	STUFF	NO-STUFF
R2U1	STUFF	NO-STUFF
R3E1	STUFF	NO-STUFF
R3E2	STUFF	NO-STUFF
R3E3	STUFF	NO-STUFF
R3E4	STUFF	NO-STUFF
R3F16	STUFF	NO-STUFF
R3F2	STUFF	NO-STUFF
R3F3	STUFF	NO-STUFF
R3F5	STUFF	NO-STUFF
R3G1	STUFF	NO-STUFF
R3G6	STUFF	NO-STUFF
R3G7	STUFF	NO-STUFF
R3G8	STUFF	NO-STUFF
R3G9	STUFF	NO-STUFF
R3N6	STUFF	NO-STUFF
R3U1	STUFF	NO-STUFF
R3U2	STUFF	NO-STUFF
R3U3	STUFF	NO-STUFF
R4B1	STUFF	NO-STUFF
R4B18	STUFF	NO-STUFF
R4B2	STUFF	NO-STUFF
R4B3	STUFF	NO-STUFF
R4N1	STUFF	NO-STUFF
R4N10	STUFF	NO-STUFF
R4N13	STUFF	NO-STUFF
R4N14	STUFF	NO-STUFF
R4N2	STUFF	NO-STUFF
R4N3	STUFF	NO-STUFF
R4N4	STUFF	NO-STUFF
R4N5	STUFF	NO-STUFF
R4N7	STUFF	NO-STUFF
R4N8	STUFF	NO-STUFF
R5B6	STUFF	NO-STUFF
R5N2	STUFF	NO-STUFF
R6A10	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R6A11	STUFF	NO-STUFF
R6M3	STUFF	NO-STUFF
R6M4	STUFF	NO-STUFF
U1F2	STUFF	NO-STUFF
U1F3	STUFF	NO-STUFF
U1G2	STUFF	NO-STUFF
U1U1	STUFF	NO-STUFF
U2U1	STUFF	NO-STUFF
U3E1	STUFF	NO-STUFF
U3E2	STUFF	NO-STUFF
U3G2	STUFF	NO-STUFF
U3G3	STUFF	NO-STUFF
U3T1	STUFF	NO-STUFF
U3V1	STUFF	NO-STUFF
U4B1	STUFF	NO-STUFF
U4B2	STUFF	NO-STUFF
U5B2	STUFF	NO-STUFF
U5B6	STUFF	NO-STUFF
U5N1	STUFF	NO-STUFF
U6A1	STUFF	NO-STUFF

PLEASE SEE BOM VARIANTS FOR STUFFING INSTUCTIONS
ON V1P2 AND STBY MARGINING

GDDR MEM. REFDES TO STUFF

REFDES	TOP ONLY (4GB)	TOP & BOT (8GB)
C5F1	STUFF	STUFF
C5U9	STUFF	STUFF
C6F3	STUFF	STUFF
C6U7	STUFF	STUFF
C7D12	STUFF	STUFF
C7E9	STUFF	STUFF
C7R6	STUFF	STUFF
C7T7	STUFF	STUFF
R5F5	STUFF	STUFF
R5T6	STUFF	STUFF
R5T7	STUFF	STUFF
R5U1	NO-STUFF	STUFF
R5U6	STUFF	STUFF
R6F5	STUFF	STUFF
R6R1	STUFF	STUFF
R6R2	STUFF	STUFF
R6T7	STUFF	STUFF
R6T8	STUFF	STUFF
R6T9	STUFF	STUFF
R6U1	NO-STUFF	STUFF
R7E1	STUFF	STUFF
R7E8	STUFF	STUFF
R7T1	NO-STUFF	STUFF
R7T6	NO-STUFF	STUFF
U5F1	STUFF	STUFF
U5U1	NO-STUFF	STUFF
U5U2	NO-STUFF	STUFF
U6F1	STUFF	STUFF
U6U1	NO-STUFF	STUFF
U7D1	STUFF	STUFF
U7E1	STUFF	STUFF
U7T1	NO-STUFF	STUFF
U7T1	NO-STUFF	STUFF

SROM MEMORY REFDES TO STUFF

REFDES	DEBUG	CPU DBG	XDK	RETAIL
C4R4	STUFF	STUFF	STUFF	NO-STUFF
R4R7	STUFF	STUFF	STUFF	NO-STUFF
R4R9	STUFF	STUFF	STUFF	NO-STUFF
R4R10	NO-STUFF	NO-STUFF	NO-STUFF	NO-STUFF
R4R11	STUFF	STUFF	STUFF	NO-STUFF
R4R12	STUFF	STUFF	STUFF	NO-STUFF

[PAGE_TITLE=COMPONENT STUFFING TABLES]

DRAWING
Thu Feb 17 10:11:24 2011

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	CORONA_XDK_4L	71/87	E	1.01

I2C REFERENCE TABLES

DIGITAL POTENTIOMETERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	256	0.007031V	W: 01011000 0X58, R: 01011001 0X59
VEDRAM	256	0.004199V	W: 01011000 0X58, R: 01011001 0X59
V5P0	256	0.011719V	W: 01011010 0X5A, R: 01011011 0X5B
V3P3	256	0.008V	W: 01011010 0X5A, R: 01011011 0X5B
VREF	256	0.007031V	W: 01011110 0X5E, R: 01011111 0X5F
VCS	256	?V	W: 01011110 0X5E, R: 01011111 0X5F
GPUPCIE	256	0.005859V	W: 01011100 0X5C, R: 01011101 0X5D
CPUPLL_1P8	256	0.007148V	W: 01011100 0X5C, R: 01011101 0X5D
V1P2STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V3P3STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V1P2	?	?V	W: 01010110 0X56, R: 01010111 0X57

STEPS/STEPSIZE TB UPDATED

ANALOG TO DIGITAL CONVERTERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
VEDRAM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
V5P0	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
V3P3	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
VCS	4096	0.000806V	W: 01001000 0X48, R: 01001001 0X49
MEM_VREF	4096	0.000806V	W: 01000110 0X46, R: 01000111 0X47
GPUPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
CPUPLL_1P8	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
V12P0	?	?V	W: 10000000 0X80, R: 10000001 0X81
TEMP SENSOR	?	?V	W: 10011100 0X9C, R: 10011101 0X9D
V5P0STBY	?	?V	W: 10011000 0X98, R: 10011001 0X99
V1P2STBY	?	?V	W: 10000110 0X86, R: 10000111 0X87
V3P3STBY	?	?V	W: 10010010 0X92, R: 10010011 0X93
V1P2	?	?V	W: 10000010 0X82, R: 10000011 0X83

STEPS/STEPSIZE TB UPDATED

CORONA DOC TRACKER

Item Id	Item Description
H101606	CORONA DOCUMENT TREE
H08945	SPEC,DC OUTPUT CORD ASSY ACCEPTANCE SPECIFICATION,DUAL BARREL
H08755	TRINITY CONSOLE ETHERNET SPECIFICATION
H08751	TRINITY CONSOLE FLASH SPECIFICATION
H08769	TRINITY CONSOLE PLL SPECIFICATION
H08757	TRINITY CONSOLE IR SPECIFICATION
H08770	TRINITY CONSOLE TILT SWITCH SPECIFICATION
H08775	TRINITY CONSOLE FPM LED DISPLAY SPEC
H100732	BORON EEPROM INITIALIZATION SPECIFICATION,SYDNEY
H09553	802.11N WI-FI MODULE SUPPLIER QUALIFICATION REQUIREMENTS
H08759	TRINITY CONSOLE V_CPUVCS REGULATOR SPECIFICATION
H08764	TRINITY CONSOLE V_MEM REGULATOR SPECIFICATION
H08765	TRINITY CONSOLE V_EDRAM REGULATOR SPECIFICATION
H08758	TRINITY CONSOLE V_CPUCORE REGULATOR SPECIFICATION
H02235	SPEC,XENON,OPTICAL DISC DRIVE ANTI PIRACY SPECIFICATION
H08938	XBOX360 OPTICAL DISC DRIVE COMPONENT SPECIFICATION,MUSTANG
H08939	XBOX360 OPTICAL DISC DRIVE INTERFACE SPECIFICATION,MUSTANG
H08753	MUSTANG HARD DRIVE COMPONENTS SPECIFICATION
H08756	TRINITY CONSOLE USB SPECIFICATION
H09169	SPECIFICATION,RJ45+AUXILIARY POWER CONNECTOR
H08676	CONSOLE USAGE MODEL AND RELIABILITY BUDGET
H08776	TRINITY CONSOLE FPM REQUIREMENTS DOCUMENT
H08754	TRINITY CONSOLE AUDIO / VIDEO SPECIFICATION
H05204	SPEC,XENON PCB SPECIFICATION,TG150
H09297	SPEC,SYSTEM FAN,HIGH SPEED PWM
H101572	SPEC,ACPT,SYS PS,135W,SMALL FORM FACTOR;2-OUTP W/FAN,1/2W
H101637	CORONA Console Security Specification
H101659	CORONA CONSOLE V_3P3STBY REGULATOR SPECIFICATION
H101660	CORONA CONSOLE V_1P2STBY REGULATOR SPECIFICATION
H101661	CORONA CONSOLE LINEAR REGULATORS SPECIFICATION
H101662	CORONA CONSOLE VR ARCHITECTURE
H101663	CORONA SYSTEM POWER BUDGET
H101664	CORONA SMC FIRMWARE REQUIREMENTS
H101665	CORONA POWER ON RESET TIMING DIAGRAM
H101667	CORONA CONSOLE SPECIFICATIONS TEMPLATE
H101502	CORONA GAME CONSOLE PRODUCTS SPECIFICATION
H101669	CORONA CONSOLE FLASH SPECIFICATION
H101670	CORONA MMC SPECIFICATION
H101671	CORONA SYSTEM BLOCK DIAGRAM
H101672	CORONA 1/2W STANDBY POWER BUDGET
H09424	VEJLE CPU DATASHEET
H08762	TRINITY CONSOLE V_5P0 REGULATOR SPECIFICATION
H101005	Wave Module Specification

[PAGE_TITLE=DOC TRACKER]

Title: Basenet Report
Design: corona
Date: Feb 17 21:27:51 2011

Base nets and synonyms for corona_lib.CORONA(@corona_lib.corona(sch_1))
Base Signal
 Location([Zone][dir])

AUD_L_OUT	33C1 37C7
AUD_RDY_BSBY	24A6 35A3
AUD_RDY_BSBY_R	24B2 24A8 62C8
AUD_RST_N	24B2 33B6
AUD_R_OUT	33B1 37C7
AUD_SPI_CLK	24A6 35A7
AUD_SPI_CLK_R	24B2 24A8 62C8
AUD_SPI_MISO	35A3 24B6
AUD_SPI_MISO_R	24B8 24B2 62C5
AUD_SPI_MOSI	24C6 35A7
AUD_SPI_MOSI_R	24B2 24C8 62C5
AUD_SSB	24A3 35A7
AUD_SSB_R	24B2 24A5 62C8
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AUD_VOUTL_R	33B3
AUD_VOUTR	33B4
AUD_VOUTR_R	33B3
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AV_MODE0_R	25C6
AV_MODE1	37C3 25C8 37C3
AV_MODE1_R	25C6
AV_MODE2	37C3 25B8 37C3
AV_MODE2_R	25B6
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BLEEDER_V12P0_C1	42B6
BLEEDER_V12P0_C2	42B6
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BORONFPMPORT_DP	26B2 38B8
BORONFPM_CLK	25A2 38A8
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BRD_TEMP_N_KSB	61B5 23A8
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BRD_TEMP_P	61B8 23C8 38A8
BRD_TEMP_P_DIODE	23C7
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BRD_TEMP_P_KSB	23A1 61B5
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CPU_CORE_HF_CLKOUT_DN	6D1
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CPU_DBG1_POST1	3A5
CPU_DBG2_POST2	3A5
CPU_DBG3_POST3	3A5
CPU_DBG4_POST4	3A5
CPU_DBG5_POST5	3A5
CPU_DBG6_POST6	3A5
CPU_DBG7_POST7	3A5
CPU_DBG8_RST0	3A5
CPU_DBG9_RST1	3A5
CPU_DBG10_RST2	3A5
CPU_DBG11_GPU_HB	3A5
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CPU_DBG13_CPUCLK1	3A5
CPU_DBG14_GPUCLK0	3A5
CPU_DBG15_GPUCLK1	3A5
CPU_DBG_RST_EN	2B7
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FLSH_DATA<0>	63C3
FLSH_DATA<7..0>	26D7 32A8 32B6 34C8
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FLSH_DATA<2>	63C3
FLSH_DATA<3>	63C1
FLSH_DATA<4>	63C3
FLSH_DATA<5>	63C1
FLSH_DATA<6>	63C3
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HDMI_TX1_DP_R	23B2
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MARGIN_VMEM_VEDRAM_AD1	55C4
MARGIN_VMEM_VREFS_BOT	57A6
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MARGIN_VREFS_AD1	57A6
MARGIN_VREFS_AS	57D4
MARGIN_VREFS_CONVST	57C4
MA_A<11..0>	12C5 14C8 15C8
MA_BA<2..0>	12C5 14C8 15C8
MA_CAS_N	12B5 14B8 15B8
MA_CKE	12B5 14B8 15B8
MA_CLK0_DN	12C5 14D8
MA_CLK0_DP	12C5 14D8
MA_CLK1_DN	12C5 15D8
MA_CLK1_DP	12C5 15D8
MA_CS0_N	12B5 14B8
MA_CS1_N	12B5 14B8 15B8
MA_DM0	12B8 14B4 15B5
MA_DM1	12C8 14B4 15B5
MA_DM2	12C8 14C4 15C5
MA_DM3	12D8 14C4 15C5
MA_DQ0	12B8 14B4 15B5
MA_DQ1	12B8 14B4 15B5
MA_DQ2	12B8 14B4 15B5
MA_DQ3	12B8 14B4 15B5
MA_DQ4	12B6 12B8 14B4 15B5
MA_DQ5	12B8 14B4 15C5
MA_DQ6	12B8 14B4 15C5
MA_DQ7	12B8 14B4 15C5
MA_DQ8	12C8 14B4 15B5
MA_DQ9	12C8 14B4 15B5
MA_DQ10	12C8 14B4 15B5
MA_DQ11	12C8 14B4 15B5
MA_DQ12	12B6 12C8 14B4 15B5
MA_DQ13	12C8 14B4 15B5
MA_DQ14	12C8 14C4 15B5
MA_DQ15	12C8 14C4 15B5
MA_DQ16	12C8 14C4 15C5
MA_DQ17	12C8 14C4 15C5
MA_DQ18	12C8 14C4 15C5
MA_DQ19	12C8 14C4 15C5
MA_DQ20	12C8 14C4 15D5
MA_DQ21	12C8 14C4 15D5
MA_DQ22	12C8 14C4 15D5
MA_DQ23	12C8 14C4 15D5
MA_DQ24	12D8 14C4 15C5
MA_DQ25	12D8 14C4 15C5
MA_DQ26	12D8 14C4 15C5
MA_DQ27	12D8 14C4 15C5
MA_DQ28	12D8 14C4 15C5
MA_DQ29	12D8 14D4 15C5
MA_DQ30	12D8 14D4 15C5
MA_DQ31	12D8 14D4 15C5
MA_RAS_N	12B5 14B8 15B8

MA_RDQS0	14B4 15B5 12B8
MA_RDQS1	14B4 15B5 12C8
MA_RDQS2	14C4 15C5 12C8
MA_RDQS3	14C4 15C5 12D8
MA_VREF0	12A7
MA_WDQS0	12A6 12B8 14B4 15B5
MA_WDQS1	12B6 12C8 14B4 15B5
MA_WDQS2	12C8 14C4 15C5
MA_WDQS3	12D8 14C4 15C5
MA_WE_N	12B5 14B8 15B8
MA_ZQ_BOT	15B5
MA_ZQ_TOP	14B5
MB_A<11..0>	12C1 16C8 17C8
MB_BA<2..0>	12C1 16B8 17B8
MB_CAS_N	12B1 16B8 17B8
MB_CKE	12B1 16B8 17B8
MB_CLK0_DN	12C1 16C8
MB_CLK0_DP	12C1 16D8
MB_CLK1_DN	12C1 17C8
MB_CLK1_DP	12C1 17D8
MB_CS0_N	12B1 16B8
MB_CS1_N	12B1 16B8 17B8
MB_DM0	12B4 16B5 17B5
MB_DM1	12C4 16B5 17B5
MB_DM2	12C4 16C5 17C5
MB_DM3	12D4 16C5 17C5
MB_DQ0	12B4 16B5 17B5
MB_DQ1	12B4 16B5 17B5
MB_DQ2	12B4 16B5 17B5
MB_DQ3	12B4 16B5 17B5
MB_DQ4	12B2 12B4 16B5 17B5
MB_DQ5	12B4 16B5 17B5
MB_DQ6	12B4 16B5 17B5
MB_DQ7	12B4 16B5 17B5
MB_DQ8	12C4 16B5 17B5
MB_DQ9	12C4 16B5 17B5
MB_DQ10	12C4 16B5 17B5
MB_DQ11	12C4 16B5 17B5
MB_DQ12	12B2 12C4 16B5 17B5
MB_DQ13	12C4 16B5 17B5
MB_DQ14	12C4 16B5 17B5
MB_DQ15	12C4 16B5 17B5
MB_DQ16	12C4 16C5 17C5
MB_DQ17	12C4 16C5 17C5
MB_DQ18	12C4 16C5 17C5
MB_DQ19	12C4 16C5 17C5
MB_DQ20	12C4 16C5 17C5
MB_DQ21	12C4 16C5 17C5
MB_DQ22	12C4 16C5 17C5
MB_DQ23	12C4 16C5 17D5
MB_DQ24	12D4 16C5 17C5
MB_DQ25	12D4 16C5 17C5
MB_DQ26	12D4 16C5 17C5
MB_DQ27	12D4 16C5 17C5
MB_DQ28	12D4 16C5 17C5
MB_DQ29	12D4 16C5 17C5
MB_DQ30	12D4 16C5 17C5

MB_DQ31	12D4 16D5 17C5
MB_RAS_N	12B1 16B8 17B8
MB_RDQS0	16B5 17B5 12B4
MB_RDQS1	16B5 17B5 12C4
MB_RDQS2	16C5 17C5 12C4
MB_RDQS3	16C5 17C5 12D4
MB_VREF0	12A3
MB_WDQS0	12A2 12B4 16B5 17B5
MB_WDQS1	12B2 12C4 16B5 17B5
MB_WDQS2	12C4 16C5 17C5
MB_WDQS3	12D4 16C5 17C5
MB_WE_N	12B1 16B8 17B8
MB_ZQ_BOT	17A5
MB_ZQ_TOP	16A5
MC_A<11..0>	13C5 18C8 19C8
MC_BA<2..0>	13C5 18B8 19B8
MC_CAS_N	13B5 18B8 19B8
MC_CKE	13C5 18B8 19B8
MC_CLK0_DN	13C5 18D8
MC_CLK0_DP	13C5 18D8
MC_CLK1_DN	13C5 19D8
MC_CLK1_DP	13D5 19D8
MC_CS0_N	13B5 18B8
MC_CS1_N	13B5 18B8 19B8
MC_DM0	13B8 18B4 19B4
MC_DM1	13C8 18B4 19B4
MC_DM2	13C8 18C4 19C4
MC_DM3	13D8 18C4 19C4
MC_DQ0	13B8 18B4 19B4
MC_DQ1	13B8 18B4 19B4
MC_DQ2	13B8 18B4 19B4
MC_DQ3	13B8 18B4 19B4
MC_DQ4	13B6 13B8 18B4 19B4
MC_DQ5	13B8 18B4 19B4
MC_DQ6	13B8 18B4 19B4
MC_DQ7	13B8 18B4 19C4
MC_DQ8	13C8 18B4 19B4
MC_DQ9	13C8 18B4 19B4
MC_DQ10	13C8 18B4 19B4
MC_DQ11	13C8 18B4 19B4
MC_DQ12	13B6 13C8 18B4 19B4
MC_DQ13	13C8 18B4 19B4
MC_DQ14	13C8 18C4 19B4
MC_DQ15	13C8 18C4 19B4
MC_DQ16	13C8 18C4 19C4
MC_DQ17	13C8 18C4 19C4
MC_DQ18	13C8 18C4 19C4
MC_DQ19	13C8 18C4 19C4
MC_DQ20	13C8 18C4 19C4
MC_DQ21	13C8 18C4 19C4
MC_DQ22	13C8 18C4 19D4
MC_DQ23	13D8 18C4 19D4
MC_DQ24	13D8 18C4 19C4
MC_DQ25	13D8 18C4 19C4
MC_DQ26	13D8 18C4 19C4
MC_DQ27	13D8 18C4 19C4
MC_DQ28	13D8 18C4 19C4

MC_DQ29	13D8 18D4 19C4
MC_DQ30	13D8 18D4 19C4
MC_DQ31	13D8 18D4 19C4
MC_RAS_N	13B5 18B8 19B8
MC_RDQS0	18B4 19B4 13B8
MC_RDQS1	18B4 19B4 13C8
MC_RDQS2	18C4 19C4 13C8
MC_RDQS3	18C4 19C4 13D8
MC_VREF0	13A7
MC_WDQS0	13B5 13B8 18B4 19B4
MC_WDQS1	13B5 13C8 18B4 19B4
MC_WDQS2	13C8 18C4 19C4
MC_WDQS3	13D8 18C4 19C4
MC_WE_N	13B5 18B8 19B8
MC_ZQ_BOT	19B5
MC_ZQ_TOP	18B5
MD_A<11..0>	13C1 20C8 21C8
MD_BA<2..0>	13C1 20C8 21B8
MD_CAS_N	13B1 20B8 21B8
MD_CKE	13C1 20B8 21B8
MD_CLK0_DN	13C1 20D8
MD_CLK0_DP	13C1 20D8
MD_CLK1_DN	13C1 21D8
MD_CLK1_DP	13D1 21D8
MD_CS0_N	13B1 20B8
MD_CS1_N	13B1 20B8 21B8
MD_DM0	13B4 20B4 21B5
MD_DM1	13C4 20B4 21B5
MD_DM2	13C4 20C4 21C5
MD_DM3	13D4 20C4 21C5
MD_DQ0	13B4 20B4 21B5
MD_DQ1	13B4 20B4 21B5
MD_DQ2	13B4 20B4 21B5
MD_DQ3	13B4 20B4 21B5
MD_DQ4	13B4 20B4 21B5
MD_DQ5	13B4 20B4 21B5
MD_DQ6	13B4 20B4 21C5
MD_DQ7	13B4 20B4 21C5
MD_DQ8	13C4 20B4 21B5
MD_DQ9	13C4 20B4 21B5
MD_DQ10	13C4 20B4 21B5
MD_DQ11	13C4 20B4 21B5
MD_DQ12	13B2 13C4 20C4 21B5
MD_DQ13	13C4 20C4 21B5
MD_DQ14	13C4 20C4 21B5
MD_DQ15	13C4 20C4 21B5
MD_DQ16	13C4 20C4 21C5
MD_DQ17	13C4 20C4 21C5
MD_DQ18	13C4 20C4 21C5
MD_DQ19	13C4 20C4 21C5
MD_DQ20	13C4 20C4 21C5
MD_DQ21	13C4 20C4 21D5
MD_DQ22	13C4 20C4 21D5
MD_DQ23	13D4 20C4 21D5
MD_DQ24	13D4 20C4 21C5
MD_DQ25	13D4 20C4 21C5
MD_DQ26	13D4 20C4 21C5

MD_DQ27	13D4 20D4 21C5
MD_DQ28	13D4 20D4 21C5
MD_DQ29	13D4 20D4 21C5
MD_DQ30	13D4 20D4 21C5
MD_DQ31	13D4 20D4 21C5
MD_RAS_N	13B1 20B8 21B8
MD_RDQS0	20B4 21B5 13B4
MD_RDQS1	20B4 21B5 13C4
MD_RDQS2	20C4 21C5 13C4
MD_RDQS3	20C4 21C5 13D4
MD_VREF0	13A3
MD_WDQS0	13B4 20B4 21B5
MD_WDQS1	13B2 13C4 20B4 21B5
MD_WDQS2	13C4 20C4 21C5
MD_WDQS3	13D4 20C4 21C5
MD_WE_N	13B1 20B8 21B8
MD_ZQ_BOT	21B5
MD_ZQ_TOP	20B5
MEM_A_VREF0	15A6 14B8 15B8
MEM_A_VREF1	14A6 14B8 15B8
MEM_B_VREF0	17A6 16B8 17B8
MEM_B_VREF1	16A6 16B8 17B8
MEM_CALA	4A6
MEM_CALB	4A6
MEM_C_VREF0	19A6 18B8 19B8
MEM_C_VREF1	18A6 18B8 19B8
MEM_D_VREF0	21A6 20B8 21B8
MEM_D_VREF1	20A6 20B8 21B8
MEM_RST	4B1 14D8 15D8 16C8 17C8 18D8 19C8 20D8 21D8
MEM_SCAN_BOT_EN	4A1 15B8 17B8 19B8 21B8
MEM_SCAN_BOT_EN_N	4A4
MEM_SCAN_EN	4A1 14B8 15B8 16B8 17B8 18B8 19B8 20B8 21B8
MEM_SCAN_TOP_EN	4A1 14B8 16B8 18B8 20B8
MEM_VREFS	57A6 57D4
MEM_VREFS_R	57A6
MMC_DV_CARD	32C5
MMC_EMBED_SEL	32C5
MMC_FLSH_ALE	32B3
MMC_FLSH_CE0_N	32B3
MMC_FLSH_CE1_N	32B3
MMC_FLSH_CLE	32B3
MMC_FLSH_DATA0	32C3
MMC_FLSH_DATA1	32C3
MMC_FLSH_DATA2	32C3
MMC_FLSH_DATA3	32C3
MMC_FLSH_DATA4	32C3
MMC_FLSH_DATA5	32C3
MMC_FLSH_DATA6	32C3
MMC_FLSH_DATA7	32C3
MMC_FLSH_READY	32B3
MMC_FLSH_RE_N	32B3
MMC_FLSH_WE_N	32B3
MMC_FLSH_WP_N	32B3

MMC_ISOLT	32C5
MMC_RSTCLK	32C5
MMC_RST_N	32C7 63C1
MMC_SD_SEL	32C5
MMC_V12	32C6
MON_V1P2STBY_A0	59A2
MON_V1P2STBY_A1	59A2
MON_V1P2_A0	60C6
MON_V1P2_A1	60C6
MON_V3P3STBY_A0	59A6
MON_V3P3STBY_A1	59A6
MON_V5P0STBY_A0	59C6
MON_V5P0STBY_A1	59C6
MON_V12P0_A0	58C6
MON_V12P0_A1	58C6
ODD_RX_DN	41A8 27B8
ODD_RX_DN_C	41A7
ODD_RX_DP	41A8 27B8
ODD_RX_DP_C	41A7
ODD_TX_DN	27A1 41A8
ODD_TX_DN_C	41A7
ODD_TX_DP	27A1 41B8
ODD_TX_DP_C	41B7
PEX_GPU_SB_L0_DN	4C2 24C7 62A6
PEX_GPU_SB_L0_DN_C	4C4
PEX_GPU_SB_L0_DP	4C2 24C7 62A6
PEX_GPU_SB_L0_DP_C	4C4
PEX_GPU_SB_L1_DN	4C2 24C7 62A6
PEX_GPU_SB_L1_DN_C	4C4
PEX_GPU_SB_L1_DP	4D2 24C7 62A6
PEX_GPU_SB_L1_DP_C	4D4
PEX_RCAL	4C6
PEX_SB_GPU_L0_DN	24C1 4C8 62A8
PEX_SB_GPU_L0_DN_C	24C3
PEX_SB_GPU_L0_DP	24C1 4C8 62A8
PEX_SB_GPU_L0_DP_C	24C3
PEX_SB_GPU_L1_DN	24D1 4C8 62A8
PEX_SB_GPU_L1_DN_C	24D3
PEX_SB_GPU_L1_DP	24D1 4C8 62A8
PEX_SB_GPU_L1_DP_C	24D3
PIX_CLK_2X_DN	22A1 4C8
PIX_CLK_2X_DN_R	22B4
PIX_CLK_2X_DP	22A1 4C8
PIX_CLK_2X_DP_R	22B4
PIX_DATA<14..0>	4C2 23D7
PMBUS_CLK	55D6 44C8 55A2 55D1 56B1 56D4 57B2 57C2 57D1 58A5 58C8 58D1 59A4 59A7 59C5 59C8 60C4 60C8 64B2
PMBUS_DATA	44C8 55A2 55D1 55D6 56B1 56D3 57A2 57C2 57D1 58A5 58C8 58D1 59A4 59A7 59C5 59C8 60C4 60C8 64B2
POR_BYPASS	22C6
POST_IN<0..4>	3C4
PSU_V12P0_EN	25A7 38A4 42B8
PSU_V12P0_EN_R	38A2
PWRSW_N	38A8 25C2 35A3
PWRSW_N_R	35B3 38A8

RESISTOR0_DN	2B7
RESISTOR0_DP	2B7
SB_GPIO<0>	24A2 62D5
SB_GPIO<0..15>	24D5
SB_GPIO<1>	24A2 62D5
SB_GPIO<2>	24A2 62C8
SB_GPIO<3>	24A2 62C5
SB_GPIO<4>	24A2 62D8
SB_GPIO<5>	24B2 62C5
SB_MAIN_PWRGD	25A8 22C2
SB_MAIN_PWRGD_R	25A6
SB_RST_N	25A7 22C1
SB_RST_N_R	22C4
SB_TCLK	63C8 24A6
SB_TDI	63C8 24A6
SB_TDO	24A6 63C8
SB_TMS	63C6 24A6
SB_TRST	63C6 24A6
SCART_RGB	24B2 37B8 62D5
SCART_RGB_OUT	37B6
SCART_RGB_OUT_R	37B7
SCART_RGB_R	37B7
SMB_CLK	22B8 25B8 55D8 61D3 62B5
SMB_CLK_EXTTEMP	61A2 61C2 61D1
SMB_CLK_EXTTEMP_R	61D2
SMB_CLK_R	62B4
SMB_DATA	22B8 25B8 55C8 61D3 62A1
SMB_DATA_EXTTEMP	61A2 61C2 61D1
SMB_DATA_EXTTEMP_R	61D2
SMB_DATA_R	62A3
SMC_CPU_CHKSTOP_DETECT	25A7 63A3
SMC_CPU_CHKSTOP_DETECT_B	63A5
SMC_DBG_EN	62B5 25C8
SMC_DBG_RXD	62A2 25C8
SMC_DBG_RXD_R	62B1 62A5
SMC_DBG_TXD	25D2 62B5
SMC_DBG_TXD_R	25D4
SMC_P0_GPIO5	25B4
SMC_PWM0	25A2 23A8
SMC_PWM1	25A2 36A6
SMC_PWM1_R	36A3
SMC_RST_N	22C1 25D8 42B3 62B1
SMC_RST_N_R	22C4
SMC_RST_XDK_N	62B3
SPDIF_OUT	27B1 37D8 39A8
SPDIF_OUT_R	27B4
SPI_CLK	62B6 26D7
SPI_MISO	26D2 62B8
SPI_MISO_R	26D4
SPI_MOSI	62B6 26D7
SPI_SS_N	62B8 26D7
SPKR_DRIVE_N	35A3
SPKR_DRIVE_P	35A3
TILTSW_N	35C3 25C2
TILTSW_N_R	35C5

TRAY_OPEN	25A7 41A1
TRAY_OPEN_R	25A6
TRAY_STATUS	41A4 25A7
TRAY_STATUS_R	41A3
USBB_D1_DN	26B4
USBB_D1_DP	26B4
V1P2STBY_ISENSE_N	53D2 59A4
V1P2STBY_ISENSE_N_R	59A3
V1P2STBY_ISENSE_P	53D2 59B4
V1P2STBY_ISENSE_P_R	59B3
V1P2_ISENSE_N	52D4 60C8
V1P2_ISENSE_N_R	60C6
V1P2_ISENSE_P	52D4 60D8
V1P2_ISENSE_P_R	60D6
V3P3STBY_ISENSE_N	53B1 59A7
V3P3STBY_ISENSE_N_R	59A6
V3P3STBY_ISENSE_P	53B1 59B7
V3P3STBY_ISENSE_P_R	59B6
V5P0STBY_CONN	38A2
V5P0STBY_ISENSE_N	38A2 59C8
V5P0STBY_ISENSE_N_R	59C6
V5P0STBY_ISENSE_P	38A2 59D8
V5P0STBY_ISENSE_P_R	59D6
V5P0_EXPPORT_RJ45	38D5
V12P0_EXPPORT_RJ45	38D5
V12P0_PWRGD	22D3 25B8 42B8
VAA_3P3STBY_USB_FET	30B5
VAA_3P3STBY_USB_FET_EN	30B5
VAA_3P3_HDMI	31C4
VAA_3P3_HDMI_FET_EN	31D2
VAA_3P3_LDO25	31B4
VCC_WAVEPORT	39B6
VDD18_OUT_CAP	30B2
VDD25_OUT_CAP	31C4
VDD_3P3_LDO18	30C2
VID_DACA_DP	23D2 37B8
VID_DACA_DP_L	37B7
VID_DACA_OUT	37B4 37D7
VID_DACB_DP	23D2 37A8
VID_DACB_DP_L	37A7
VID_DACB_OUT	37A4 37D7
VID_DACC_DP	23D2 37B4
VID_DACC_DP_L	37B3
VID_DACC_OUT	37B1 37D7
VID_DACD_DP	23D2 37A4
VID_DACD_DP_L	37A3
VID_DACD_OUT	37A1 37C7
VID_HSYNC_OUT	37B1 37C7
VID_HSYNC_OUT_R	23C3 37B3
VID_VSYNC_OUT	37B3 37C7
VID_VSYNC_OUT_R	23C3 37B5
VREG_1P2STBY_EN	53C6
VREG_1P2STBY_FB	53B1 59D5
VREG_1P2STBY_FB_CHIP	53C5
VREG_1P2STBY_FB_D	59D4
VREG_1P2STBY_FB_MID	59D5 53B1
VREG_1P2STBY_FB_R	53B3

VREG_1P2STBY_SW	53C5
VREG_1P2_EN	25C8 52C8
VREG_1P2_EN_R	25C6
VREG_1P2_FB	52C4 60D4
VREG_1P2_FB_MID	60C4 52C4
VREG_1P2_PWRGD	52C8
VREG_3P3STBY_EN	53A7
VREG_3P3STBY_FB	53A1 59D1
VREG_3P3STBY_FB_CHIP	53A4
VREG_3P3STBY_FB_D	59D3
VREG_3P3STBY_FB_MID	59C1 53A1
VREG_3P3STBY_FB_R	53A3
VREG_3P3STBY_SW	53A5
VREG_CPU1_VCC	45B7
VREG_CPU2_VCC	45D7
VREG_CPUCORE_PWRGD	44D1 25A7
VREG_CPUPLL_1P8_FB	52A5 58A8 58D1
VREG_CPUPLL_1P8_FB_MID	58D1 52A5
VREG_CPUPLL_ADJUST	52A8
VREG_CPUPLL_B3	58C2
VREG_CPUPLL_PCIE_AS	58A7
VREG_CPUPLL_PCIE_CONVST_N	58A7
VREG_CPUPLL_R	52A7
VREG_CPU_ALERT_N	44C2
VREG_CPU_BST1	45B5
VREG_CPU_BST1_R	45A5
VREG_CPU_BST2	45D5
VREG_CPU_BST2_R	45D5
VREG_CPU_COMP	44C4
VREG_CPU_COMP_R	44A6
VREG_CPU_CSCOMP	44C8 64B2
VREG_CPU_CSCOMP_R	44B6
VREG_CPU_CSREF	44C8 64B2
VREG_CPU_CSSUM	44C8 64B2
VREG_CPU_DRVH1	45A5
VREG_CPU_DRVH2	45C5
VREG_CPU_DRVL1	45A5
VREG_CPU_DRVL2	45C5
VREG_CPU_DRV_EN	44C1 45C8
VREG_CPU_EN	25A8 44D8
VREG_CPU_FAULT_N	44C2
VREG_CPU_FB	44A6 44C4
VREG_CPU_FBRTN	44B3 44C4
VREG_CPU_ILIMITFS	44B4
VREG_CPU_IMON	44C2
VREG_CPU_IREF	44C4
VREG_CPU_OD1_N	44C2
VREG_CPU_PHASE1	45A1 44C8
VREG_CPU_PHASE1_R	44C4
VREG_CPU_PHASE2	45C1 44C8
VREG_CPU_PHASE2_R	44C4
VREG_CPU_PWM1	44C1 45A8
VREG_CPU_PWM2	44C1 45C8
VREG_CPU_RAMPADJ	44D4
VREG_CPU_RAMPADJ_R	44D5
VREG_CPU_RT	44C2
VREG_CPU_SW1_R	45A2

VREG_CPU_SW2_R	45C3
VREG_CPU_SW3	44C4
VREG_CPU_SW4	44C4
VREG_CPU_TRDET	44C4
VREG_CPU_TRDET_R	44A6
VREG_CPU_VCC	44C1 44D1
VREG_CPU_VCC3_3P3	44D3
VREG_CPU_VID<6..1>	43C2 44D1 64C2
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VREG_EFUSE_VOUT	52A2
VREG_GPUPCIE_B1	58C4
VREG_GPUPCIE_FB	52C1 58A8 58D5
VREG_GPUPCIE_FB_MID	58D5 52C1
VREG_PCIEX_ADJUST	52C3
VREG_PCIEX_R	52C2
VREG_V3P3_BST	48C5
VREG_V3P3_CF1	56A6
VREG_V3P3_COMP	48A8
VREG_V3P3_COMP_C	48A7
VREG_V3P3_DH	48C5
VREG_V3P3_DL	48B5
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VREG_V3P3_FB	48B1 56D1
VREG_V3P3_FB_A3	56D4
VREG_V3P3_FB_MID	48A1 56C1
VREG_V3P3_FB_MID_R	56C4
VREG_V3P3_FB_R	56A4
VREG_V3P3_ILIM	48B5
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VREG_V3P3_ISENSE_N	48C1 56A7
VREG_V3P3_ISENSE_P	48C1 56A7
VREG_V3P3_PGND	48B5
VREG_V3P3_PWRGD	48D1 25C1
VREG_V3P3_RAMP	48D5
VREG_V3P3_RSENSE	48C3
VREG_V3P3_SS	48A7
VREG_V3P3_SW	48C5
VREG_V3P3_SW_S	48C3
VREG_V3P3_TRK	48C7
VREG_V3P3_V5P0_FREQ	47B7
VREG_V3P3_V5P0_SYNC	47C7
VREG_V3P3_V5P0_VCCO	47D1 48D8
VREG_V3P3_V5P0_VDL	47D7
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VREG_V5P0_SEL_B1	46C6
VREG_V5P0_SEL_B2	46C5
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VREG_V12P0_ISENSE_N_R	58C6
VREG_V12P0_ISENSE_P	38B1 58D8
VREG_V12P0_ISENSE_P_R	58D6
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VREG_VCS_FB_MID_R	57A4
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VREG_VCS_HDRV_R	51C4
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VREG_VCS_IOUT2	57C6
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VREG_VCS_ISENSE_P	51C1 57C8
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VREG_VCS_NC1	51C6
VREG_VCS_NC2	51C6
VREG_VCS_OCP	51C6
VREG_VCS_SS_SD_N	51B6
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VREG_VCS_VOUT_L	51B3
VREG_VCS_VP	51C6
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VREG_VMEM_TRK	50C7
VREG_VMEM_VEDRAM_SYNC	49C7
VREG_VMEM_VEDRAM_VCCO	49D1 50D8
VREG_VMEM_VEDRAM_VDL	49D7
VREG_V_CPUCORE_S	44A8
VSS_PLLA	31B4
VSS_PLLB	31B4
V_1P2STBY_R	53C4
V_3P3STBY_LED_R	63A1
V_3P3STBY_R	53A4
V_3P3_LED_R	63A1
V_3P3_VREF_CPUPLL_PCIE	58B7
V_3P3_VREF_V5P0_V3P3	56B3
V_3P3_VREF_VCS	57D5
V_3P3_VREF_VMEM_VEDRAM	55B3
V_5P0STBY_LED_R	63A2
V_5P0_LED_R	63A2
V_12P0_DET	22C6
V_12P0_IN	38A2
V_12P0_LED_R	63A2
V_AUD	33D6
V_AUD_BIAS	33C4
V_AUD_FILT_N	33A4
V_AUD_FILT_P	33C4
V_AUD_FLYN_N	33B4

V_AUD_FLYN_P	33B4
V_AUD_FLYP_N	33C4
V_AUD_FLYP_P	33C4
V_AVIP	37D3 39A8 40A8
V_CPU_CORE_HF_GNDA_PLL	6A4
V_CPU_CORE_HF_VDDA_PLL	6B4
V_CPU_GNDA_RNG	6B4
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V_CPU_PVDDA_PEX	6C4
V_CPU_PVSSA_ED	6B4
V_CPU_PVSSA_HS	6C4
V_CPU_PVSSA_MEM	6C4
V_CPU_PVSSA_PEX	6C4
V_CPU_VDDA_RNG	6B4
V_CPU_VDD_VTTA	6A4
V_ENET_CT	38C4
V_EXPPORT_DUAL1	39D2
V_EXPPORT_DUAL2	39C2
V_EXPPORT_DUAL3	39B2
V_FAN1	36C5
V_GAMEPORT1	39D6
V_GAMEPORT2	39C6
V_GPU_GNDA_PLL	6A4
V_GPU_VDDA_PLL	6A4
V_HDD	41D2
V_IR	35C6
V_RST_OK	22D3
V_VREG_1P2	52C7
V_VREG_1P2_ADJUST	52C7
V_VREG_1P2_IN	52C8
V_VREG_1P8PLL	52B7
V_VREG_CPU	43B2 44D8 45D8
V_VREG_GPUPCIE	52D3
V_VREG_STBY_VIN	53C7
V_VREG_V3P3_V5P0	47D1 26B3 31C1 48D8
V_VREG_VCS	51C5
V_VREG_VMEM_VEDRAM	49D1 50D8
WAVEPORT_DN	26C2 39B8
WAVEPORT_DP	26C2 39B8
WSS_CNTL0	24B2 37C8 62D8
WSS_CNTL1	24B2 37C8 62D5
WSS_CNTL_B	37C7
WSS_CNTL_E	37C7
WSS_CNTL_OUT	37C6
WSS_CNTL_OUT_R	37C7
XTAL_IN	22C6
XTAL_OUT	22C6

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C7A4	CAPN_603	[38]
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C7B3	CAP_P_TH	[43]
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C7B8	CAP_P_TH	[49]

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C7P2	CAPN_603	[44]
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D2G1	LED_SM	[63]
D2G2	LED_SM	[63]
D4A1	DIODE_SOT23	[36]
D4B1	LED_SM	[63]
D4P1	LED_SM	[63]
D5A1	LED_SM	[63]
D5B1	DIODE_SOT23	[45]
D6A1	LED_SM	[63]
D6B1	DIODE_SOT23	[45]
D7A1	LED_SM	[63]
DB1B1	DBPAD_LARGE-TP	[63]
DB1C1	DBPAD_LARGE-TP	[63]
DB1D1	DBPAD_LARGE-TP	[63]
DB1D2	DBPAD_LARGE-TP	[63]
DB1E1	DBPAD_TP	[42]
DB1E2	DBPAD_TP	[25]
DB1R1	DBPAD_TP	[32]
DB2B1	DBPAD_LARGE-TP	[63]
DB2B2	DBPAD_LARGE-TP	[63]
DB2B3	DBPAD_LARGE-TP	[63]
DB2C1	DBPAD_TP	[25]
DB2C2	DBPAD_TP	[22]
DB2C3	DBPAD_LARGE-TP	[63]
DB2C4	DBPAD_LARGE-TP	[63]
DB2C5	DBPAD_LARGE-TP	[63]
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DB2E1	DBPAD_TP	[52]
DB2E2	DBPAD_TP	[25]
DB2E3	DBPAD_TP	[25]
DB2E4	DBPAD_LARGE-TP	[63]
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DB2G1	DBPAD_TP	[48]
DB2G2	DBPAD_TP	[47]
DB2G3	DBPAD_TP	[25]
DB2G4	DBPAD_TP	[47]
DB2G5	DBPAD_LARGE-TP	[63]
DB2P1	DBPAD_TP	[25]
DB3A1	DBPAD_TP	[37]
DB3A2	DBPAD_TP	[33]
DB3A3	DBPAD_TP	[33]
DB3A4	DBPAD_TP	[33]
DB3B1	DBPAD_TP	[33]
DB3C1	DBPAD_TP	[25]
DB3C2	DBPAD_TP	[53]
DB3C3	DBPAD_TP	[25]
DB3C4	DBPAD_LARGE-TP	[63]

DB3D1	DBPAD_TP	[22]
DB3D2	DBPAD_TP	[22]
DB3D3	DBPAD_TP	[22]
DB3E1	DBPAD_TP	[52]
DB3E2	DBPAD_LARGE-TP	[63]
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DB3R3	DBPAD_TP	[25]
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DB3R6	DBPAD_TP	[22]
DB3R7	DBPAD_TP	[22]
DB4B1	DBPAD_TP	[51]
DB4B2	DBPAD_LARGE-TP	[63]
DB4C1	DBPAD_TP	[51]
DB4C2	DBPAD_TP	[52]
DB4C3	DBPAD_LARGE-TP	[63]
DB4D1	DBPAD_LARGE-TP	[63]
DB4E1	DBPAD_TP	[52]
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DB4R1	DBPAD_TP	[5]
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DB5B1	DBPAD_TP	[53]
DB5B2	DBPAD_TP	[51]
DB5B3	DBPAD_TP	[51]
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DB5M3	DBPAD_TP	[53]
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DB6M2	DBPAD_TP	[38]
DB6M3	DBPAD_TP	[38]
DB6N1	DBPAD_TP	[38]
DB6R1	DBPAD_TP	[43]
DB6R2	DBPAD_TP	[43]
DB7C1	DBPAD_TP	[44]
DB7C2	DBPAD_TP	[44]

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DB7F2	DBPAD_TP	[50]
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DB7P2	DBPAD_TP	[44]
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EG1A2	ESDGUARD_402	[39]
EG1A3	ESDGUARD_402	[39]
EG1A4	ESDGUARD_402	[39]
EG1A5	ESDGUARD_402	[39]
EG1A6	ESDGUARD_402	[39]
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EG1A8	ESDGUARD_402	[39]
EG1B1	ESDGUARD_402	[41]
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EG1B3	ESDGUARD_402	[41]
EG1B4	ESDGUARD_402	[41]
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EG6G2	ESDGUARD_402	[39]
EG7G1	ESDGUARD_402	[39]
EG7G2	ESDGUARD_402	[39]
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FB2M1	FERRITE_603	[38]
FB2R1	FERRITE_603	[30]
FB3A1	FERRITE_603	[33]
FB3A2	FERRITE_603	[33]
FB3P1	FERRITE_603	[31]
FB3P2	FERRITE_603	[31]
FB3P3	FERRITE_603	[31]
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FB5R3	FERRITE_603	[6]
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FB5T3	FERRITE_603	[6]
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FT1R4	FTPAD_TP	[32]
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FT1U2	FTPAD_TP	[35]
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FT6M1	FTPAD_TP	[38]
FT6N1	FTPAD_TP	[64]
FT6R2	FTPAD_TP	[43]
FT6V1	FTPAD_TP	[64]
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FT7N1	FTPAD_TP	[38]
FT7N2	FTPAD_TP	[64]
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FT7P7	FTPAD_TP	[2]
FT7P8	FTPAD_TP	[2]
FT7U1	FTPAD_TP	[50]
J1A1	WAVERECEPTACLE_TH	[39]
J1A2	USBTRIPLE_TH	[39]
J1B1	1X7SATA_TH	[41]
J1B2	1X7SATA_TH	[41]
J1B3	1X4HDR_TH	[41]
J1D1	1X5HDR_TH	[26]
J1F1	1X2HDR_TH	[35]
J2A1	TRINITYRJ45AUX_TH	[38]
J2C1	2X5HDR10_TH	[62]
J2C2	2X13SOFTTOUCH_SM	[62]
J2C3	2X7HDR14_TH	[62]
J2F1	1X3HDR_TH	[63]
J3A1	HDMI_1X19HDR	[40]
J3E1	PCIEXMIDBUS_SM	[62]
J3E2	2X3HDR_TH	[63]
J4A1	TOSLINK_TX_TH	[39]
J4A2	XENONAVIP_TH	[37]
J4A3	2X6HDR2_TH	[41]
J4C1	2X4HDR_TH	[63]
J4C2	2X5HDR_TH	[63]
J4C3	2X3HDR_TH	[63]
J4D2	1X3HDR_SM	[62]
J5B1	2X2HDR_TH	[55]

J5G2	XENONRF_BORON_TH	[38]
J6A5	1X4HDR_TH	[36]
J6G1	USBDUALHORIZONTAL_TH	[39]
J7A1	TRINITYPWR_TH	[38]
L1F1	INDUCTOR_SM	[48]
L2B1	INDUCTOR_TH	[47]
L2F1	INDUCTOR_TH	[47]
L4A1	INDUCTOR_1210	[37]
L4A2	INDUCTOR_1210	[37]
L4A3	INDUCTOR_1210	[37]
L4A4	INDUCTOR_1210	[37]
L4B1	INDUCTOR_TH	[51]
L4F1	INDUCTOR_TH	[49]
L5A1	INDUCTOR_1210	[53]
L5B1	INDUCTOR_1210	[53]
L5B2	INDUCTOR_SM	[53]
L5C1	INDUCTOR_TH	[51]
L6B1	INDUCTOR_TH	[43]
L6C1	IND_2MODE_SM	[45]
L6C2	IND_2MODE_TH	[45]
L7B1	INDUCTOR_TH	[49]
L7F1	INDUCTOR_TH	[50]
LB2B1	LABEL_SM	[65]
MTG1B1	STD_MTG_HOLE_TH	[65]
MTG1G1	STD_MTG_HOLE_TH	[65]
MTG4D1	STD_MTG_HOLE_TH	[65]
MTG4F1	STD_MTG_HOLE_TH	[65]
MTG4G1	STD_MTG_HOLE_TH	[65]
MTG6D1	STD_MTG_HOLE_TH	[65]
MTG6F1	STD_MTG_HOLE_TH	[65]
MTG7G1	STD_MTG_HOLE_TH	[65]
Q1F1	SHUNT_3PIN_SOT23	[56]
Q1N1	MBT3904DUAL_SOT	[46]
Q1T1	NPN_SOT23	[42]
Q1T2	NPN_SOT23	[42]
Q2F1	FET_VREG_DPAK_G1D2S3	[47]
Q2F2	FET_VREG_DPAK_G1D2S3	[47]
Q2F3	SHUNT_3PIN_SOT23	[56]
Q2P1	FET_SOT23	[31]
Q2R1	FET_SOT23	[30]
Q3A1	MBT3904DUAL_SOT	[37]
Q3F1	FET_VREG_DPAK_G1D2S3	[49]
Q3M1	PNP_SOT23	[37]
Q3R1	FET_ZGATE_P_SOT23	[61]
Q4A1	NPN_SOT23	[36]
Q4B1	ADR510_SOT23	[57]
Q4C1	NPN_SOT23	[63]
Q4C2	NPN_SOT23	[63]
Q4F1	FET_VREG_DPAK_G1D2S3	[49]
Q4G1	PNP_SOT23	[23]
Q5A2	PNP_DPAK369C	[36]
Q5B1	FET_VREG_DPAK_G1D2S3	[51]
Q5C1	FET_VREG_DPAK_G1D2S3	[45]
Q5C2	FET_VREG_DPAK_G1D2S3	[51]
Q5C3	FET_VREG_DPAK_G1D2S3	[45]
Q6A3	PNP_2C_SOT223	[42]
Q6B1	FET_VREG_DPAK_G1D2S3	[45]
Q6B2	FET_VREG_DPAK_G1D2S3	[45]
Q6C1	FET_VREG_DPAK_G1D2S3	[45]
Q6C2	FET_VREG_DPAK_G1D2S3	[45]
Q6M2	FET_SOT23	[42]
Q6M3	NPN_SOT23	[42]
Q7G1	FET_VREG_DPAK_G1D2S3	[50]
Q7G2	FET_VREG_DPAK_G1D2S3	[50]
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R1D1	RESN_402	[34]
R1D2	RESN_402	[34]
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R1E22	RESN_402	[48]
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R1N1	RESN_402	[46]
R1N2	RESN_402	[46]
R1N3	RESN_402	[46]
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R1T3	RESN_1206	[42]
R1T4	RESN_805	[47]
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R2F7	RESN_805	[47]
R2F8	RESN_402	[56]
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R2G2	RESN_1206	[47]
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R2V3	RESN_402	[35]
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R3A3	RESN_402	[37]
R3A4	RESN_402	[37]
R3A5	RESN_402	[37]
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R3A8	RESN_402	[33]
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R7T7	RESN_402	[4]
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RT1B2	THERMISTOR_1206	[41]
RT2A1	THERMISTOR_1206	[38]
RT2M1	THERMISTOR_1206	[39]
RT2M2	THERMISTOR_1206	[39]
RT3A1	THERMISTOR_1206	[37]
RT3A2	THERMISTOR_1812	[38]
RT6G1	THERMISTOR_1206	[39]
RT7V1	THERMISTOR_1206	[39]
ST1E1	SHORT_TRACE	[48]
ST1F1	SHORT_TRACE	[48]
ST1F2	SHORT_TRACE	[48]
ST1F3	SHORT_TRACE	[48]
ST1U1	SHORT_TRACE	[48]
ST2D1	SHORT_TRACE	[53]
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ST2U1	SHORT_TRACE	[47]
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ST3C6	SHORT_TRACE	[53]
ST3F1	SHORT_TRACE	[49]

ST4B1	SHORT_TRACE	[52]
ST4B2	SHORT_TRACE	[52]
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ST4F2	SHORT_TRACE	[49]
ST4F4	SHORT_TRACE	[49]
ST4R1	SHORT_SM	[61]
ST4R2	SHORT_SM	[61]
ST4U1	SHORT_TRACE	[49]
ST5A1	SHORT_TRACE	[53]
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ST5B2	SHORT_TRACE	[53]
ST5C1	SHORT_TRACE	[51]
ST5C3	SHORT_TRACE	[51]
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ST6D2	SHORT_SM	[44]
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ST6V2	SHORT_TRACE	[50]
ST7A1	SHORT_TRACE	[38]
ST7A2	SHORT_TRACE	[38]
ST7F1	SHORT_SM	[50]
ST7F2	SHORT_TRACE	[50]
ST7F3	SHORT_TRACE	[50]
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STP3D1	STP_TP	[64]
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STP5D2	STP_TP	[64]
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STP6C2	STP_TP	[64]
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STP7C1	STP_TP	[64]
STP7C2	STP_TP	[64]
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STP7C6	STP_TP	[64]
STP7C7	STP_TP	[64]
STP7E1	STP_TP	[64]
STP7E2	STP_TP	[64]
STP7N1	STP_TP	[64]
U1B1	SI4501DY_SO8	[46]
U1D1	2X8RCPT_SM	[63]
U1E1	ADP1877_LCC32	[47]
U1E1	ADP1877_LCC32	[48]
U1E2	NAND_TSOP	[34]
U1E3	PS8200_LGA51	[32]
U1F1	FET_VREG_DUAL_1_SO-8	[48]
U1F2	AD7991_SOT23	[56]
U1F3	REF3333_SC70	[56]
U1F4	TRSET_9920_TH	[35]
U1T1	NAND_2CE_TSOP48	[32]
U1U1	AD5252_TSSOP	[56]
U2U1	AD8213_MSOP10	[56]
U2V1	SN74LVC1G14_SC70	[63]
U3A1	AUDIODAC_CSS4354_WM1824_QFN25	[33]
U3B1	LD39100_DFN6	[52]
U3D1	KSB_PBGA404	[22]
U3D1	KSB_PBGA404	[23]
U3D1	KSB_PBGA404	[24]
U3D1	KSB_PBGA404	[25]
U3D1	KSB_PBGA404	[26]
U3D1	KSB_PBGA404	[27]
U3D1	KSB_PBGA404	[30 30]
U3D1	KSB_PBGA404	[31]
U3E1	AD7992_MSOP10	[58]
U3E2	AD5252_TSSOP	[58]
U3G1	ADP1877_LCC32	[49]
U3G1	ADP1877_LCC32	[50]
U3G2	AD7991_SOT23	[55]
U3G3	REF3333_SC70	[55]
U3G4	ISD2130_QFN21	[35]
U3N1	INA219_SOT23-8	[60]
U3R1	tmp441_SOT23-8	[61]
U3T1	REF3333_SC70	[58]
U3V1	AD5252_TSSOP	[55]
U3V2	AD8213_MSOP10	[55]
U4A1	BAV99DUAL_SOT363	[37 37]
U4A2	BAV99DUAL_SOT363	[37 37]
U4B1	AD5252_TSSOP	[57]
U4B2	AD7992_MSOP10	[57]
U4B3	IR3638_SSOP	[51]
U4B4	MCP4661_QFN16	[60]
U4E1	NCP1117_DPAK	[52]
U4E2	NCP1117_SOT223	[52]
U4M1	BAV99DUAL_SOT363	[37 37]
U4M2	BAV99DUAL_SOT363	[37 37]
U4P1	AT25020A_SOI8	[5]
U4P2	LD39015_SOT23-5	[52]
U4R1	tmp423_SOT23-8	[61]
U5A1	TPS62590_DFN6	[53]
U5A2	TPS62220_SOT23-5	[53]
U5A3	MCP4661_QFN16	[59]
U5B1	AD7992_MSOP10	[57]
U5B2	AD8213_MSOP10	[57]
U5B5	MOSDRIVER_SOI8	[45]
U5B6	REF3333_SC70	[57]
U5E1	VALHALLA_1_BGA_2	[2]
U5E1	VALHALLA_1_BGA_2	[3]
U5E1	VALHALLA_1_BGA_2	[4]
U5E1	VALHALLA_1_BGA_2	[5]
U5E1	VALHALLA_1_BGA_2	[6]
U5E1	VALHALLA_1_BGA_2	[7 7 7 7 7]
U5E1	VALHALLA_1_BGA_2	[8 8 8]
U5E1	VALHALLA_1_BGA_2	[12 12]
U5E1	VALHALLA_1_BGA_2	[13 13]
U5F1	GDDR136_1GBIT_BGA136	[18 18]
U5M1	INA219_SOT23-8	[59]
U5N2	INA219_SOT23-8	[59]
U5N3	INA219_SOT23-8	[59]
U5U1	GDDR136_1GBIT_BGA136	[19 19]
U5U2	74LVC1G06_SC70	[4]
U6A1	INA219_SOT23-8	[58]
U6B1	MOSDRIVER_SOI8	[45]
U6F1	GDDR136_1GBIT_BGA136	[20 20]
U6G1	IR_WHOLDER_TH	[35]
U6U1	GDDR136_1GBIT_BGA136	[21 21]
U7C1	NCP4201_LCC40	[44]
U7D1	GDDR136_1GBIT_BGA136	[16 16]
U7E1	GDDR136_1GBIT_BGA136	[14 14]
U7R1	GDDR136_1GBIT_BGA136	[17 17]
U7T1	GDDR136_1GBIT_BGA136	[15 15]
Y3D1	CRYSTAL_SM	[22]